THE SWITCH

SWITCH TO 5"/8" DOUBLE DENSITY

LNDoubler 5/8

FEATURES

- 5- and 8-inch* disk drives
- Single- & double-density
- Any size and density in any mix
- Read Model I, II* and III disks
- 5- or 8-inch* system disk
- Single & double sided disk drives
- DOS+ 3.3.9 included, with Disk BASIC.
- 6 month warranty
- Up to 3.75 megabytes online
- Easy installation – plug-in & run
- Analog phase lock loop data separation
- Precision write precompensation
- Regulated power supply
- Guaranteed operation at 4MHz
- All contacts gold plated
- Solder masked & silk screened
- Runs under DOS+ 3.3.9, TRSDOS 2.3, NEWDOS 2.1, NEWDOS/80 1.0, LDOS, NEWDOS/80 2.0, and ULTRADOS
- Reads 40- and 35-track disks on 80-track drives
- FD1791 controller (1 your FD1771
- Fits Model I expansion interfaces
- Fits LNW expansion interfaces
- Track configurations to 80-tracks
- 5 inch disk storage increased to:
  161,280 bytes – 35-track SS/DD
  322,560 bytes – 35-track DS/DD
  184,320 bytes – 40-track SS/DD
  368,640 bytes – 40 track DS/DD
  368,640 bytes – 80-track SS/DD
  737,280 bytes – 80-track DS/DD
- 8 inch disk storage increased to:
  591,360 bytes – 77-track SS/DD
  1,182,720 bytes – 77-track DS/DD

SS: single-sided DS: double-sided
SD: single-density DD: double-density

COMPLETE – The *LNDoubler 5/8*, switches your Model I or LNW-80 into the most versatile computer you can own. The LNDoubler's switch allows you to boot from 5- or 8-inch system disks, and it's accessible from outside the interface. The *LNDoubler 5/8* comes with a double-density disk operating system (DOS+ 3.3.9), complete with BASIC and utility programs . . . ready to run your software NOW!

VERSATILE – Whether you want single-sided, double-sided, single- or double-density, 5- or 8-inch operation, complete versatility is here today! Any combination of 5- and 8-inch disk storage is possible with the *LNDoubler 5/8*. Each of your present 40-track, single-sided 5-inch drives will store up to 184,320 bytes (formatted storage) – that's an 80% increase in storage capacity for only half the cost of just one disk drive. With three 8-inch double-density, double-sided drives your Model I will have 3.75 Megabytes of online storage – that's more storage than a Model II or Model III!

ADVANCED – The *LNDoubler 5/8* is the most technically advanced, tested and reliable double-density board you can buy. The *LNDoubler 5/8* has more features, more options and more software support than any other product of its kind.

EASY TO INSTALL – The *LNDoubler 5/8* is easy to install. There are no traces to cut, no wiring to do, just a screwdriver and a few minutes of your time is all that is required. The instructions are fully illustrated for all interfaces. In minutes you will be 'up-and-running', and enjoying your computer as never before.

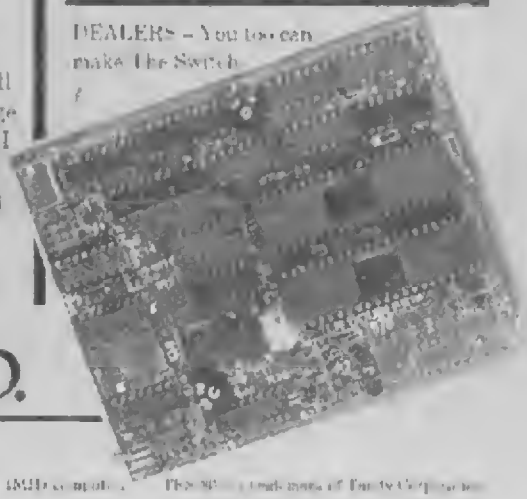
COMPARE – Compare features, compare quality, compare value, and make the SWITCH today!

Immediate delivery from stock – at your dealer NOW for only

$199.95 without DOS

$219.95 with DOS

DEALERS – You too can make The Switch



LNW Research Corp.

2620 WALNUT Tustin, CA. 92680 (714) 641-5550 (714) 544-5744

*5" & 8" operation requires special cable, ** Double density requires 3.58MHz CPU speed-up modification in LNW-80 (MHz compatible). The "80" is a trademark of Radio Shack for its

LNDOUBLER 5/8

The ultimate in double density adapter units

USER MANUAL VERSION 1.Ø
Ø8/29/81

 LNW RESEARCH CORPORATION

CONTENTS

The LNDOUBLER 5/8 switches your TRS80* MODEL I or LNW80 computer into the most versatile computer you can own.Whether you want single sided,double sided,single or double density,5 or 8 inch disk operation,any combination of disk storage is possible with the LNDOUBLER 5/8. Each of your present 40 track single sided disk drives will store up to 184,320 bytes (formatted)-thats an 80% increase! The LNDOUBLER 5/8 even allows you to BOOT from an 8" system disk with a flip of a switch.The LNDOUBLER 5/8 is compatible with all software available for 5" single and double density,8" single and double density written for the TRS80.

The LNDOUBLER 5/8 is easy to install.There are no traces to cut,no soldering or wiring.Just unplug the floppy controller IC (FD1771) from your interface,install the FD1771 into the LNDOUBLER 5/8,and just plug the LNDOUBLER 5/8 into the interface.In just a few minutes you'll be enjoying your computer as never before.

The LNDOUBLER 5/8 is the most technically advanced,tested and reliable double density board you can own.The LNDOUBLER 5/8 has more features,more capabilities, and more software support than any product of it's kind.

FEATURES

* RELIABLE OPERATION GUARANTEED WITH ALL 5.25" and 8" DISK DRIVES
* SINGLE AND DOUBLE DENSITY OPERATION
* 5.25" AND 8" IN ANY MIX
* READ MODEL I,II,III DISKS
* 5.25" AND 8" SYSTEM DISKS
* ANALOG PHASE LOCK LOOP DATA SEPARATION
* PRECISION WRITE PRECOMPENSATION
* REGULATED SUPPLY FOR VCO AND ALIGNMENT CIRCUITS
* GUARANTEED OPERATION WITH ALL TRS80 EXPANSION INTERFACE UNITS
* ALL GOLD CONTACTS
* GUARANTEED OPERATION AT 4.0 MHZ CPU SPEED
* EASY INSTALLATION
* COMPATIBLE WITH ALL SINGLE,DOUBLE AND 8" DRIVE SOFTWARE
* FIVE INCH DISK STORAGE INCREASED TO :
  - 161,280 bytes- 35 track ss/dd
  - 322,560 bytes- 35 track ds/dd
  - 184,320 bytes- 40 track ss/dd
  - 368,640 bytes- 40 track ds/dd
  - 368,640 bytes- 80 track ss/dd
  - 737,280 bytes- 80 track ds/dd

* EIGHT INCH DISK STORAGE INCREASED TO:
  - 335,104 bytes- 77 track ss/sd
  - 670,208 bytes -77 track ds/sd
  - 591,360 bytes -77 track ss/dd
  - 1,182,720 bytes -77 track ds/dd

ss: single sided ds: dual sided
sd: single density dd: double density

MEDIA AND DRIVE REQUIREMENTS

Since the LNDOUBLER 5/8 will work with virtually any drive and any media, it may be tempting to use (for example) low cost single density single sided 35 track diskettes with 8Ø track,double density double sided drives.On the other hand, experimentation to find out which diskettes work the best, may lead to the conclusion that any diskettes will work. For this reason we at LNW RESEARCH make the following suggestions:

1.Use double density rated disk drives. Single density drives may work,but the proper operation in double density cannot be guaranteed for the life of the drive.
2.Use diskettes rated according to their use
3.Check diskettes for wear periodically
4.Clean and align your disk drive(s) according to the manufacturer's recommendations.

REQUIRED ACCESSORIES FOR 5" DOUBLE DENSITY,8" AND SPECIAL SOFTWARE APPLICATIONS

All existing TRS8Ø MOD I single density software will run unmodified in SINGLE DENSITY with the LNDOUBLER 5/8 installed. In order to use double density and 8" drive capabilities, special software is required. In order to connect an eight inch disk drive to your system, a special cable adapter circuit board and an eight inch disk drive cable (5Ø cond.) is required. Some eight inch disk drive software requires a special "wait cable" (stk# 1Ø97). Some eight inch disk drives require that the "write current" line on the disk drive be driven when using these drives in double density above track 43.In order to do this another small cable is needed. This cable is called the "TG43 CABLE" (stk#1Ø97).Shugart Disk drives DO NOT NEED THIS CABLE.Check the data sheets on your drive to determine if your drive needs this signal.

The hardware/software configuration information is summarized in the following table,and ordering information for the various accessories is included at the rear of the manual

DOS	5.25" SD	5.25" DD	8" SD	8" DD
Dosplus 3.2d	X	S		
Dosplus 3.38d	X	S	X(1)	X(1,4)
Dbldos	X	S		
F.E.C. T8/OS	S		X(1,2)	
LDOS 5.Ø	S	S		
Omikron CP/M	S		S(1,2)	
Newdos8Ø 1.Ø	S	S(3)	X(1,2)	
Newdos8Ø 2.Ø	S	S	S(1)	X(1,4)
Vtos 4.Ø	S	S(3)		

NOTES:

X= non system disk

S= system or non system disk

1= requires 8" cable adapter (stk#1Ø96) and 8" drive cable (stk#1Ø99)

2= requires "wait cable" (stk#1Ø97)

3= requires Double Zap II from Software etc.

4= requires CPU speed to > 3.5 mhz or LNW8Ø computer
SEE PAGE 21 for details concerning speed up kits

SPECIAL NOTE

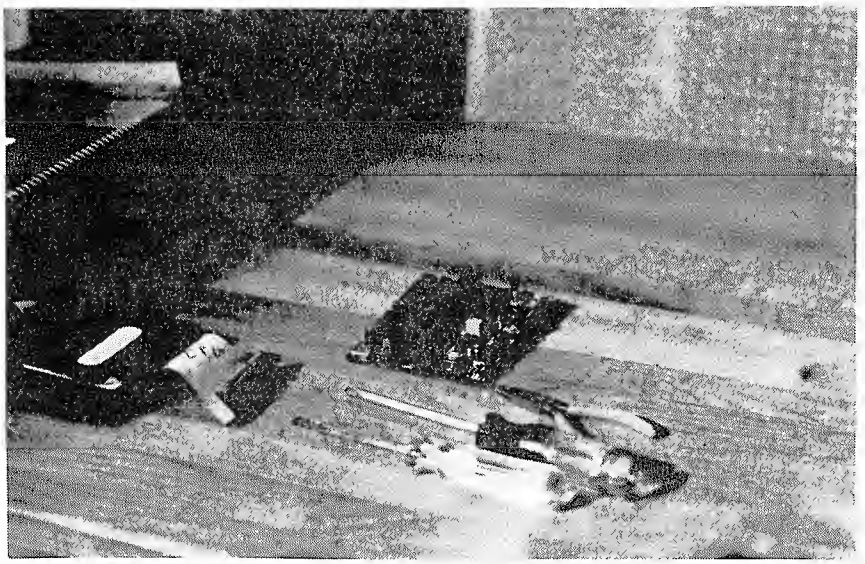
BEFORE ATTEMPTING TO INSTALL THE LNDOUBLER 5/8 INTO YOUR INTERFACE, MAKE sure THAT YOUR INTERFACE IS FUNCTIONING PROPERLY. OPENING YOUR INTERFACE DURING THE LIMITED 9Ø (18Ø FOR LNW INTERFACE) DAY WARRANTY PERIOD MAY VOID YOUR WARRANTY. EXERCISE YOUR WARRANTY RIGHTS IF NECESSARY PRIOR TO INSTALLING THE LNDOUBLER

TEST YOUR INTERFACE

To test your interface and provide a "test diskette" for our initial power up of the LNDOUBLER 5/8,make a "backup" of a single density DOS SYSTEM disk.DO NOT attempt to BOOT the double density system disk (Dosplus) without the LNDOUBLER 5/8 installed. If you are not able to correctly backup a single density SYSTEM disk DO NOT attempt to install the LNDOUBLER 5/8. It cannot fix defective interface units! After backing up the single density SYSTEM disk attempt to BOOT this disk. If it boots correctly set it aside for the initial power up with the LNDOUBLER 5/8. Proceed to INSTALLATION INSTRUCTIONS.

INSTALLATION INSTRUCTIONS

TOOLS REQUIRED:
- Small slotted screwdriver
- Medium phillips screwdriver
- Needle nose pliers or tweezers
- Large clean work space



CAUTION

THE FD1771 FLOPPY CONTROLLER IC WHICH YOU WILL BE REQUIRED TO HANDLE DURING THE INSTALLATION OF THE LNDOUBLER 5/8 IS SENSITIVE TO STATIC ELECTRICITY AND CAN EASILY BE DAMAGED BY A STATIC DISCHARGE. BREAKING THE PINS OF THE FD1771 WILL ALSO CAUSE PERMANENT DAMAGE TO THE PART. WE MAKE THE FOLLOWING RECOMMENDATION CONCERNING THE HANDLING OF THE FD1771:

1. Work in an area that is NOT CARPETED
2. Do not wear clothes that will generate static
3. Have all tools close at hand before handling the FD1771
4. Use great care when removing and installing the FD1771 to not bend or break the delicate pins

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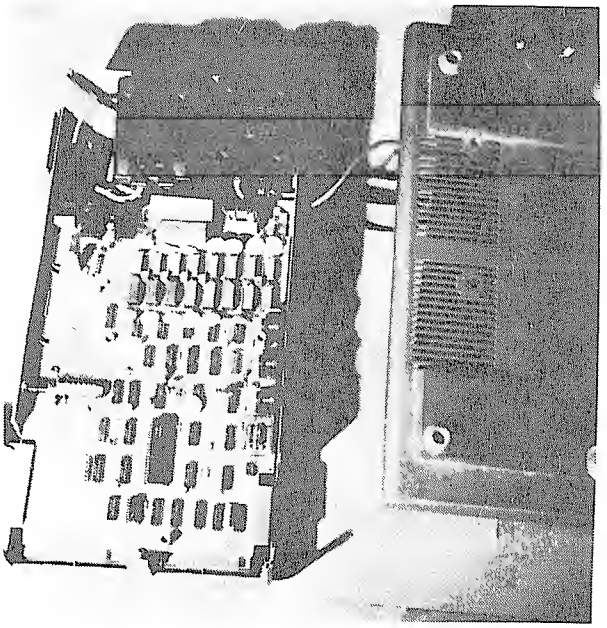
Installation instructions are provided for the two different expansion interface units for the TRS8Ø- the Tandy and the LNW interface.

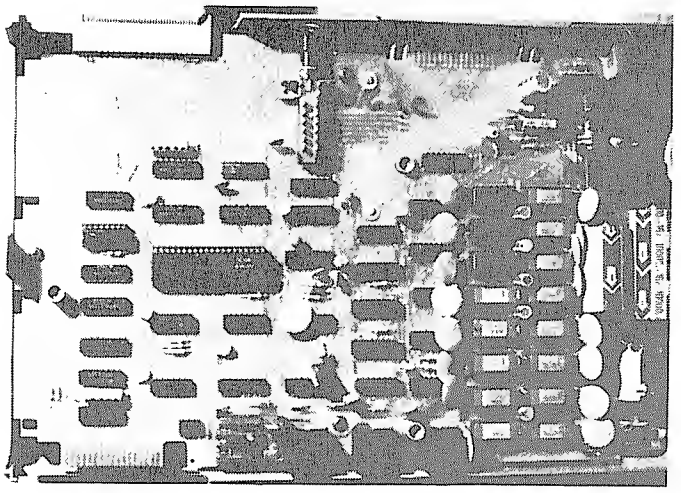
TANDY INTERFACE

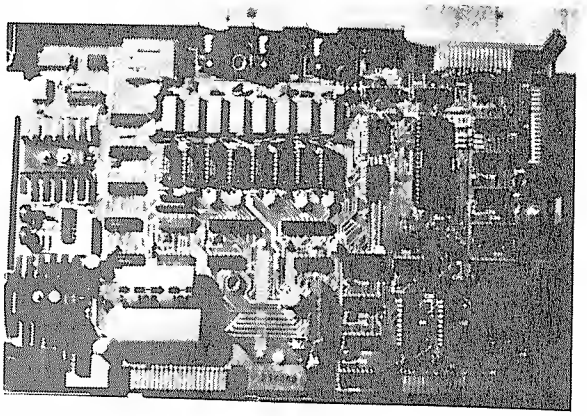
Disconnect the interface from the computer. Unplug the interface from the AC power, disconnect all cables from the interface (printer,RS232,and floppy disk,etc.). Turn the interface upside down such that the rubber feet face upward. You will notice six (6) phillips-head screws recessed into the plastic bottom of the interface case. Loosen each screw completely but don't remove them from the bottom panel.

Carefully lift the entire bottom panel away and set it beside the interface exercising care not to lose the mounting screws. Note that the screws are of different lengths.



Refer to the following photographs to identify your type of expansion interface. There are two different designs from Tandy ,the one on the left was their original interface, hence "OLD" and the one on the left is the newer of their designs and we refer to it as "NEW". Proceed to instructions provided for the type of interface which you own.

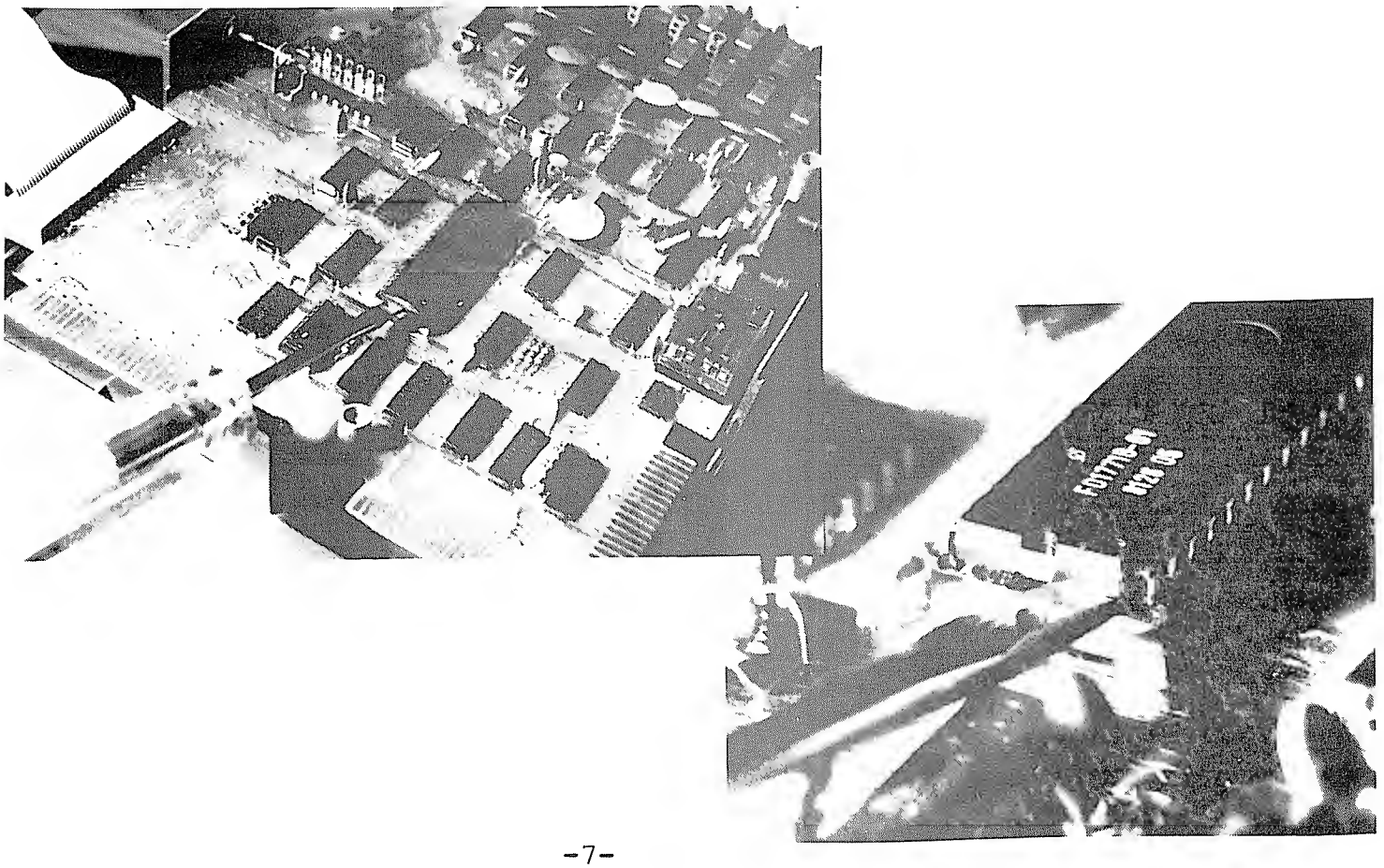




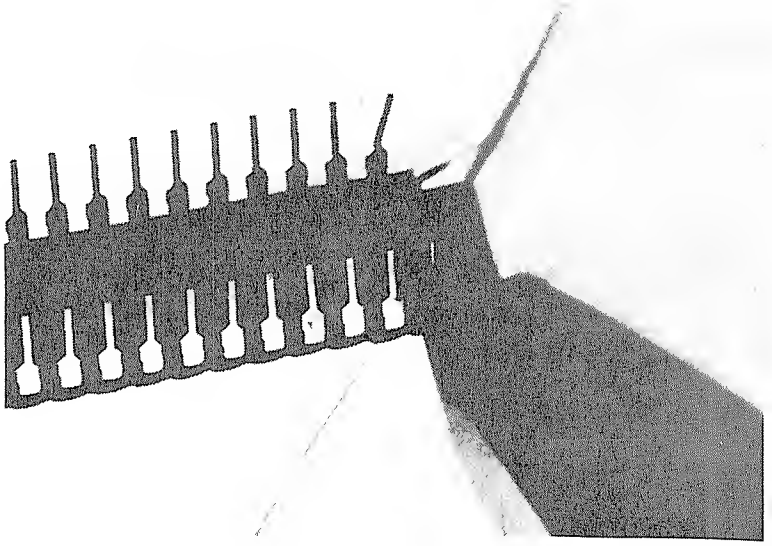
OLD EXPANSION INTERFACE

Observe the location of the floppy controller IC (the large black IC with 40 pins marked FD1771) located at position Z34. Note that the "notch" on the IC faces the center of the circuit board.

Carefully remove the the FD1771 by inserting the small screwdriver between the FD1771 and the socket that it is installed in, and pry it gently on each side. Refer to the following photos.



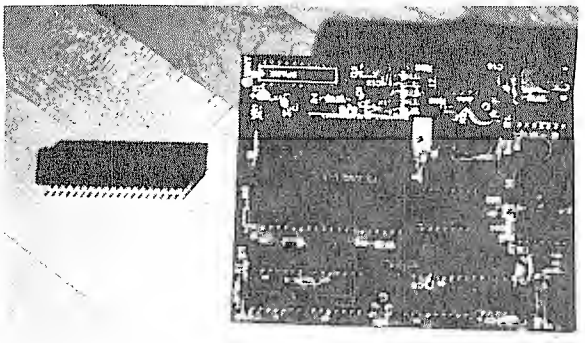
Should a lead become bent as in the next photo, use the pair of needle nose pliers or tweezers to carefully bend the pins back in place. Do not use excessive force or bend the lead back and forth too many times as the leads are delicate and can easily break.

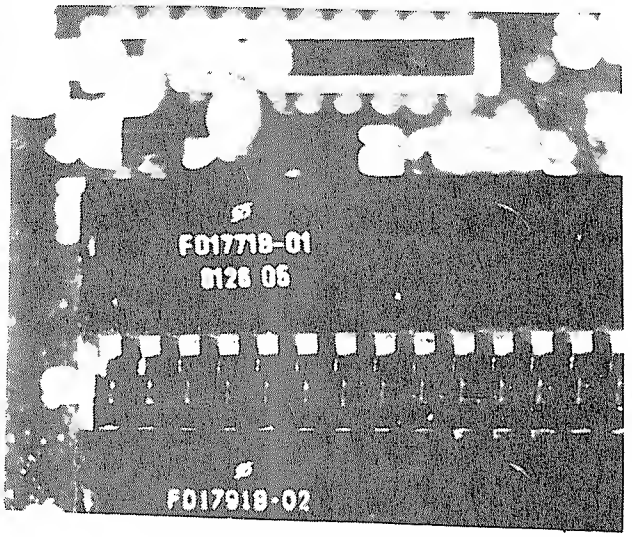


Now install the FD1771 in the socket (IC1Ø) provided on the LNDOUBLER 5/8.

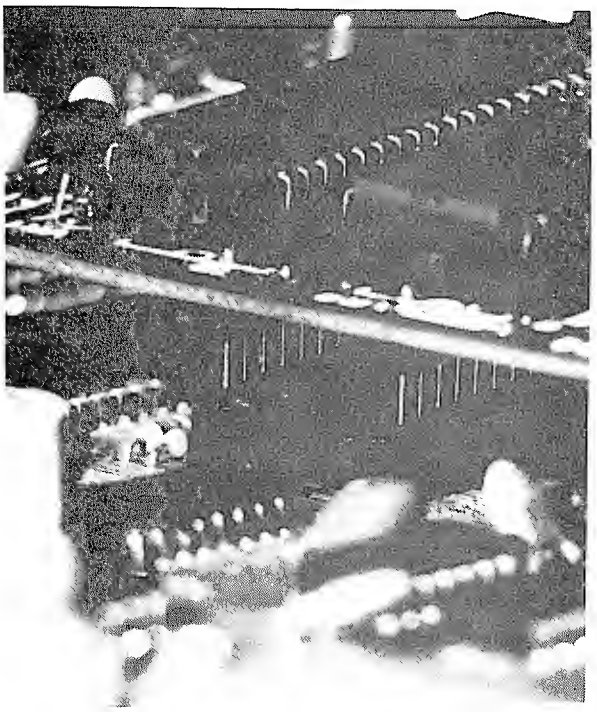
Use extreme care to insure that all 4Ø pins seat properly into the socket. The notch on the FD1771 should face the outside of the LNDOUBLER 5/8.

Inspect the seating of the FD1771 in its socket by holding the LNDOUBLER 5/8 board with the notch side of the 1771 facing you. Look between the bottom of the IC and the top of the socket and inspect the two rows of pins of the IC. If a pin is bent, carefully remove the FD1771 and bend the lead straight with the needle nose pliers or the tweezers. Reinstall the FD1771 into the socket.



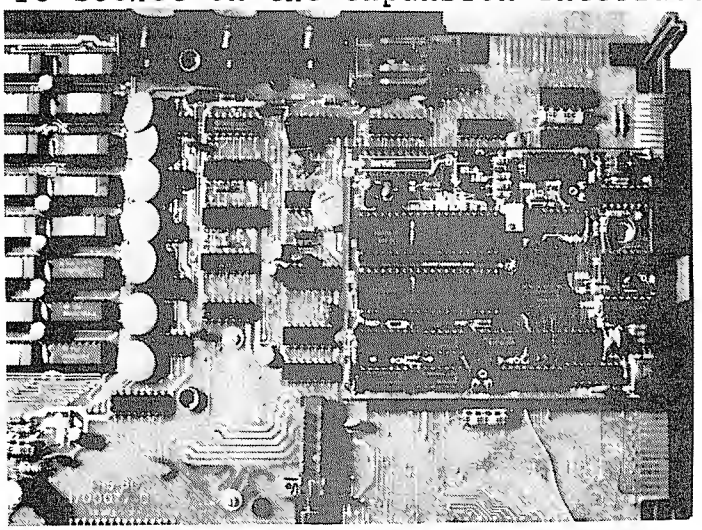


Prepare to install the LNDOUBLER 5/8 by inspecting the area on the interface near the socket and observe the area for components which might obstruct installation. Carefully reposition any components. Remove the protective foam block on the pins of the LNDOUBLER 5/8. Position the LNDOUBLER 5/8 above the socket and guide the pins of the LNDOUBLER 5/8 into the socket. Refer to the following photo.



Note that there is a small round hole on the LNDOUBLER 5/8 which allows a support on the expansion interface case to fit through.

Gently press the LNDOUBLER 5/8 into the socket. Now inspect the installation of the LNDOUBLER 5/8 making sure that all the pins are seated in the socket. If the LNDOUBLER 5/8 will not seat properly due to obstruction by a component which cannot be repositioned easily,it may be necessary to RAISE the LNDOUBLER 5/8 in its socket. This can be accomplished by installing a 40 pin dip IC socket between the LNDOUBLER 5/8 pins and the IC socket on the expansion interface.



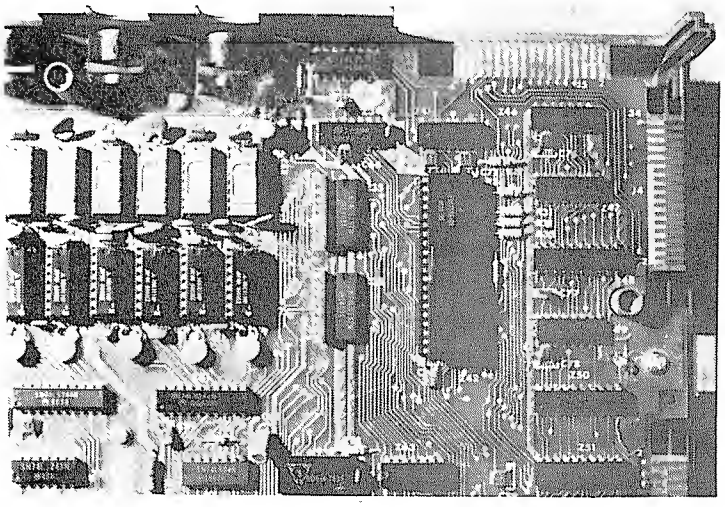
Before closing up, note the switch on the outside corner of the LNDOUBLER 5/8. It is accesible from the outside of the interface, but you must make sure you know what position it is set to before closing up the interface. SET THE SWITCH TO THE "5" POSITION. A detailed explanation of the operation of this switch is included in a later section of this manual.

Now carefully position the case bottom panel over the interface, guiding the 6 screws into their 6 plastic supports on the case. Tighten the 6 screws completely.

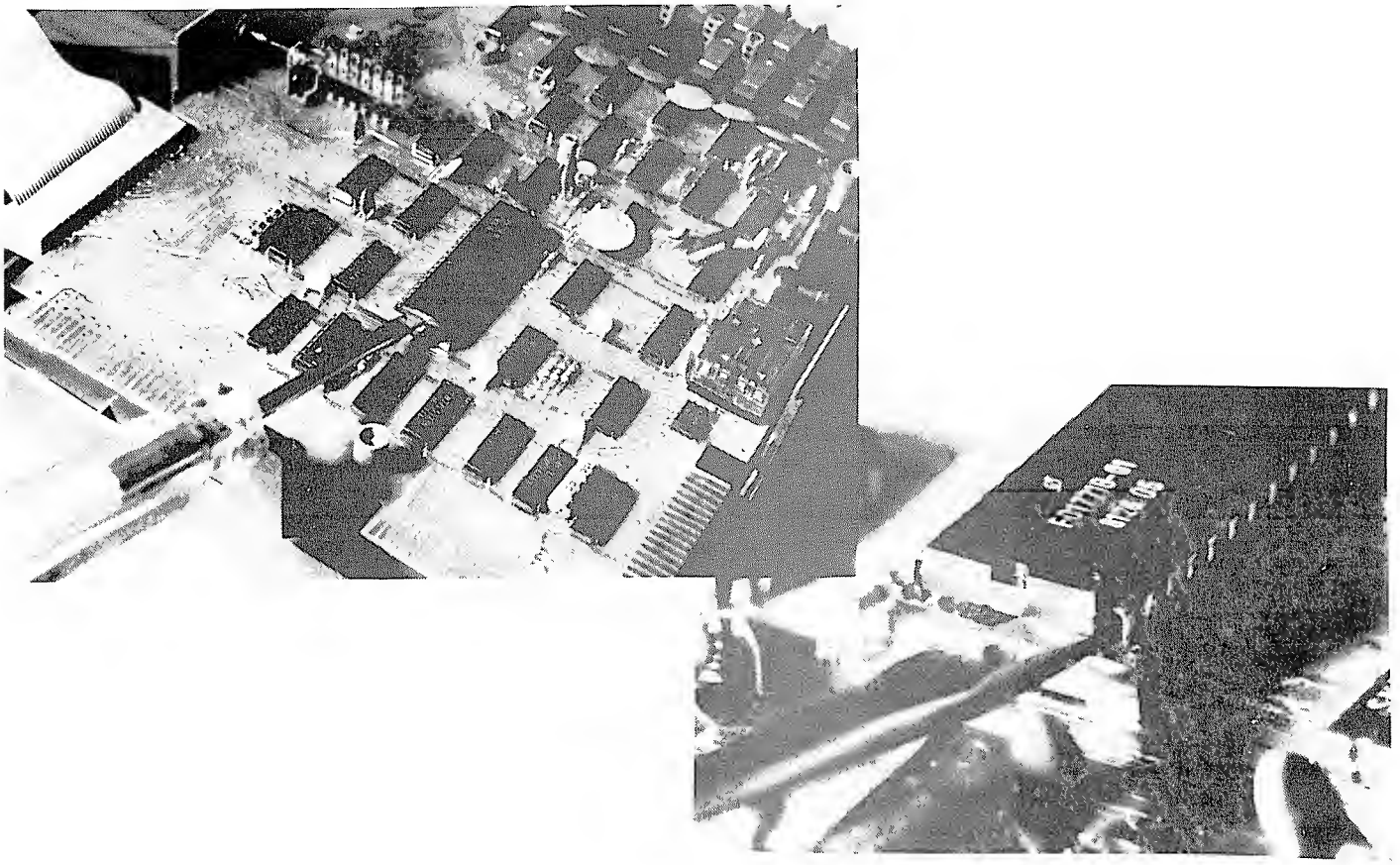
Observe the opening in the interface that the 5/8 switch is visible. Using some sort of label or tape, mark the outside of the case in such a way as to identify the setting of the switch for the "5" position. Proceed to the section entitled "POWERING UP FOR THE FIRST TIME".

NEW EXPANSION INTERFACE

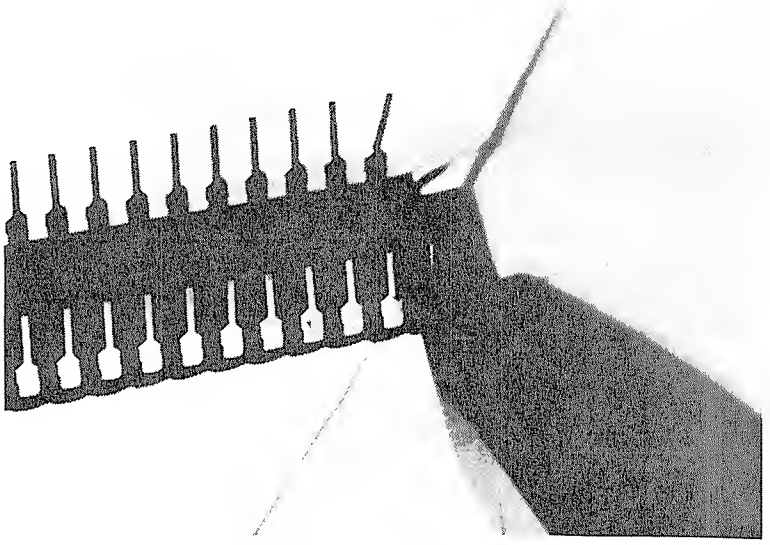
Note the location of the floppy controller IC (FD1771),the large black 40 pin IC at location Z42. The notch on the FD1771 should face Z41 and the connector for the Floppy disk drives.



Carefully remove the the FD1771 by inserting the small screwdriver between the FD1771 and the socket that it is installed in, and pry it gently on each side. Refer to the following photos.



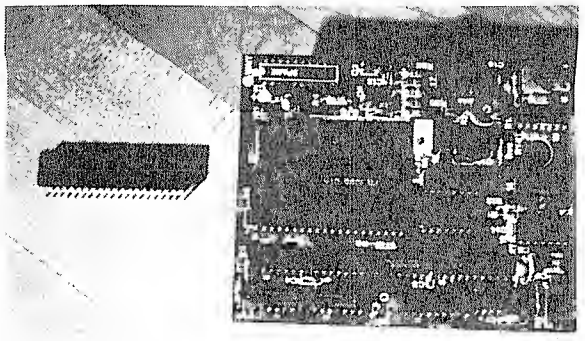
Should a lead become bent as in the next photo, use the pair of needle nose pliers or tweezers to carefully bend the pins back in place. Do not use excessive force or bend the lead back and forth too many times as the leads are delicate and can easily break.

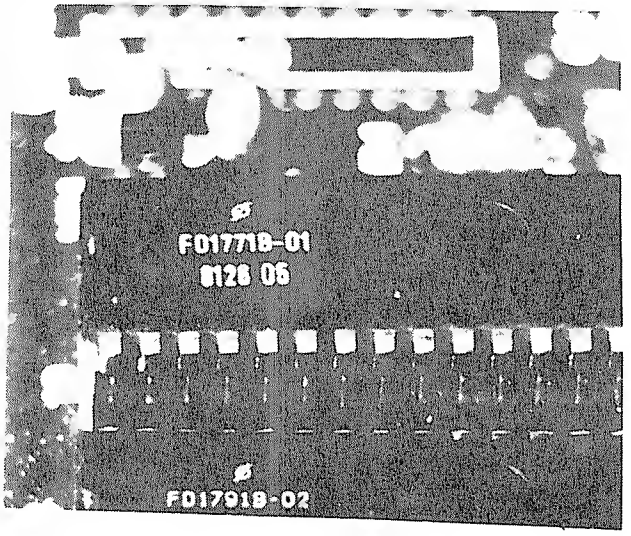


Now install the FD1771 in the socket (IC1Ø) provided on the LNDOUBLER 5/8.

Use extreme care to insure that all 4Ø pins seat properly into the socket. The notch on the FD1771 should face the outside of the LNDOUBLER 5/8.

Inspect the seating of the FD1771 in its socket by holding the LNDOUBLER 5/8 board with the notch side of the 1771 facing you. Look between the bottom of the IC and the top of the socket and inspect the two rows of pins of the IC. If a pin is bent, carefully remove the FD1771 and bend the lead straight with the needle nose pliers or the tweezers. Reinstall the FD1771 into the socket.





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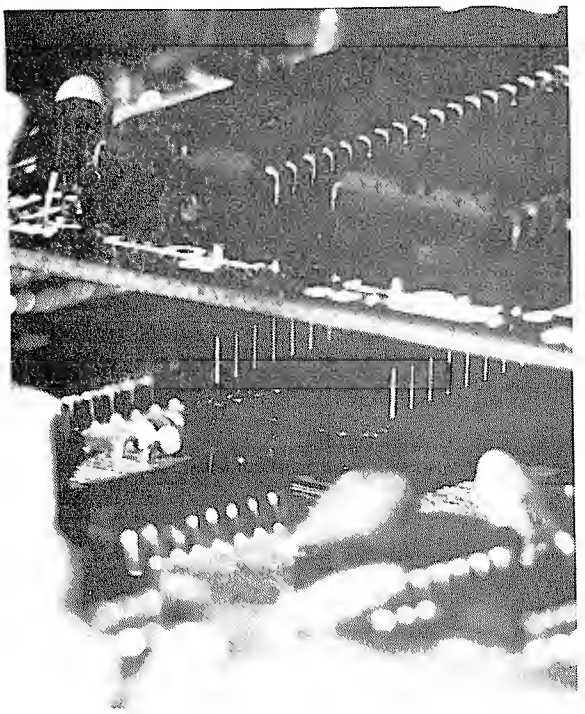
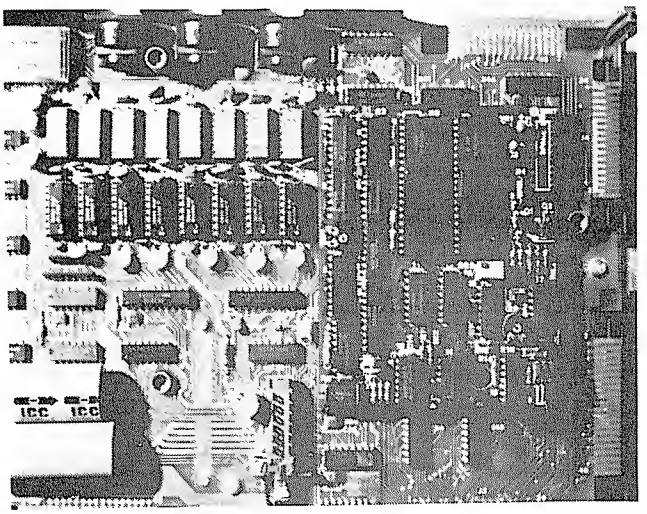


Gently press the LNDOUBLER 5/8 into the socket. Now inspect the installation of the LNDOUBLER 5/8 making sure that all the pins are seated in the socket. If the LNDOUBLER 5/8 will not seat properly due to obstruction by a component which cannot be repositioned easily,it may be necessary to RAISE the LNDOUBLER 5/8 in its socket. This can be accomplished by installing a 40 pin dip IC socket between the LNDOUBLER 5/8 pins and the IC socket on the expansion interface.



Before closing up, note the switch on the outside corner of the LNDOUBLER 5/8. It is accesible from the outside of the interface, but you must make sure you know what position it is set to before closing up the interface. SET THE SWITCH TO THE "5" POSITION. A detailed explanation of the operation of this switch is included in a later section of this manual.

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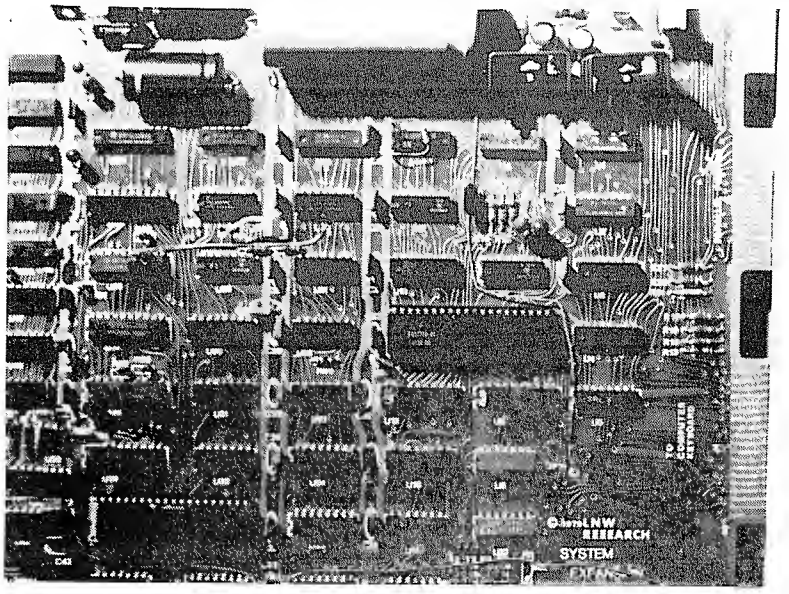
Observe the opening in the interface that the 5/8 switch is visible. Using some sort of label or tape, mark the outside of the case in such a way as to identify the setting of the switch for the "5" position. Proceed to the section entitled "POWERING UP FOR THE FIRST TIME".

Remove the two top mounting and two bottom mounting screws which secure the case top to the SYSTEM EXPANSION base. Remove the case top gently, noting that the front panel LED pilot lamp is wired to the system expansion circuit board. Position the case top upside down beside the chassis base. Remove the four circuit board mounting screws located on the edges of the system expansion circuit board. Gently position the circuit board component side up and remove the polarized power supply connector at J1 (near the large capacitors). Remove the circuit board away from the chassis and set it down on the inside of the top panel with the component side up. Since the component leads are sharp , handle the board with care and only by the edges. Also do not set the board down on any delicate surface or furniture as scratches will result.

Note the location of the floppy controller IC at U14. The "notch" on the 1771 should face C22 or the inside of the circuit board. See below:



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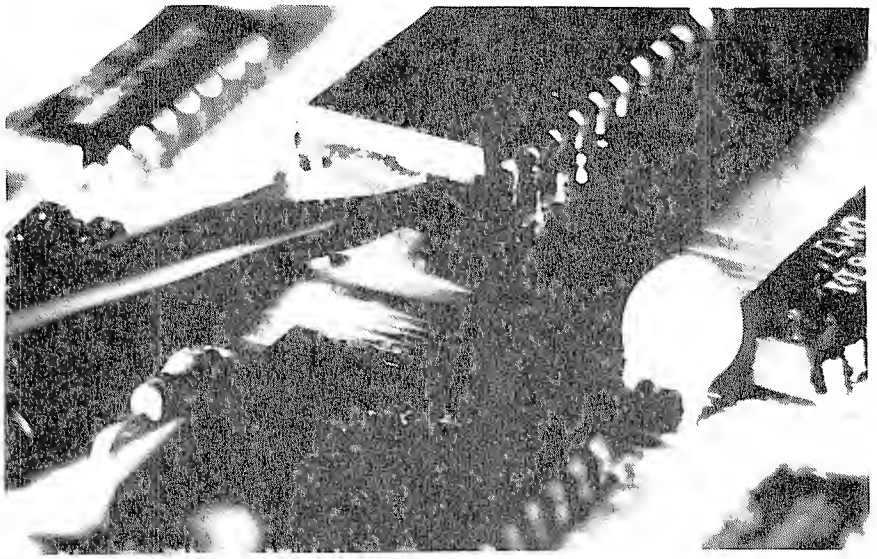
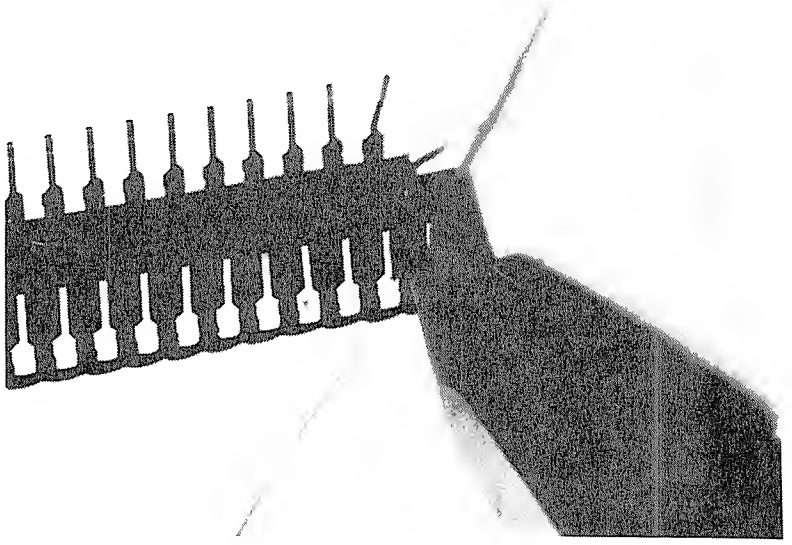


Should a lead become bent as in the next photo, use the pair of needle nose pliers or tweezers to carefully bend the pins back in place. Do not use excessive force or bend the lead back and forth too many times as the leads are delicate and can easily break.



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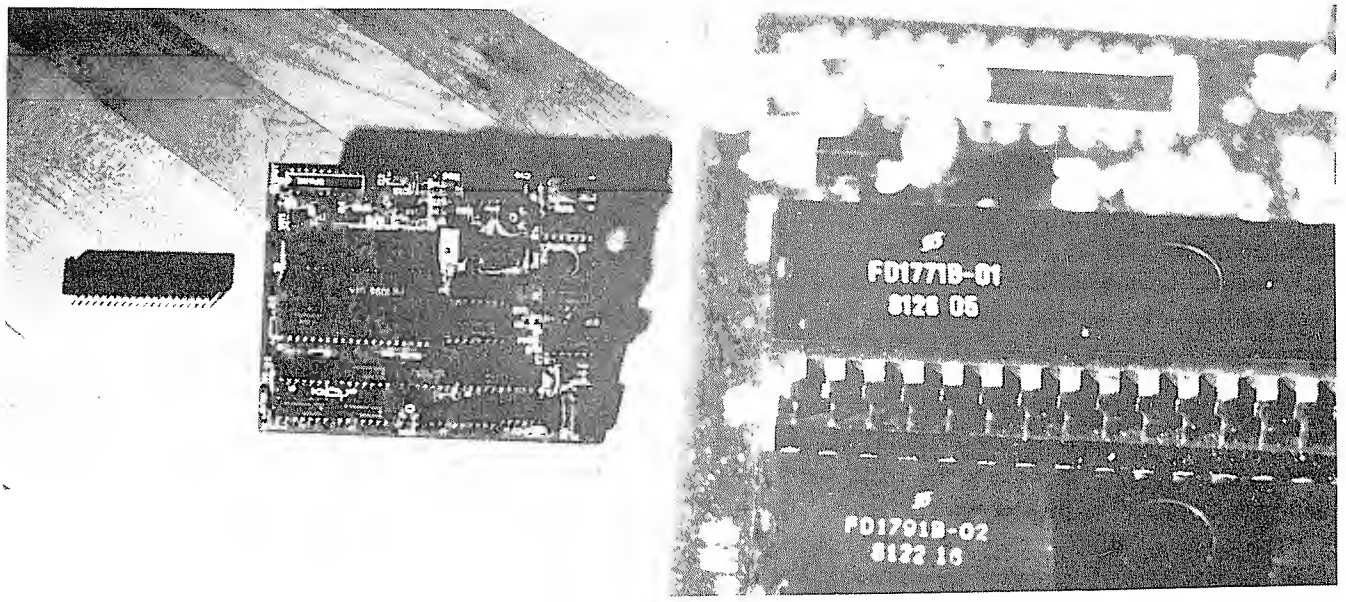
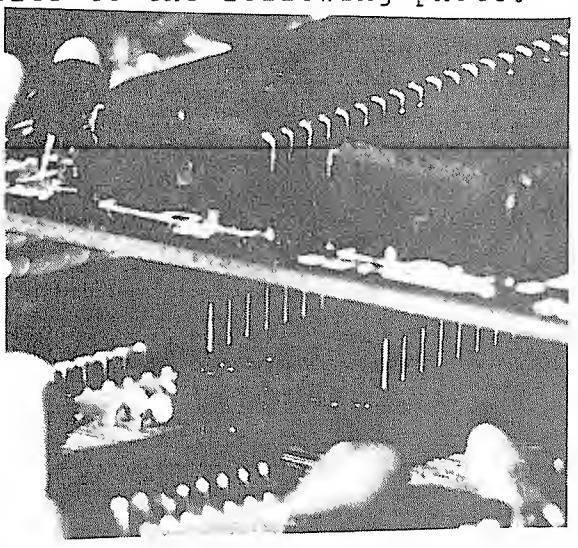
Use extreme care to insure that all 4Ø pins seat properly into the socket. The notch on the FD1771 should face the outside of the LNDOUBLER 5/8.

Inspect the seating of the FD1771 in its socket by holding the LNDOUBLER 5/8 board with the notch side of the 1771 facing you. Look between the bottom of the IC and the top of the socket and inspect the two rows of pins of the IC. If a pin is bent, carefully remove the FD1771 and bend the lead straight with the needle nose pliers or the tweezers. Reinstall the FD1771 into the socket.



Prepare to install the LNDOUBLER 5/8 by inspecting the area on the interface near the socket and observe the area for components which might obstruct installation. Carefully reposition any components. Remove the protective foam block on the pins of the LNDOUBLER 5/8. Position the LNDOUBLER 5/8 above the socket and guide the pins of the LNDOUBLER 5/8 into the socket. Refer to the following photo.



Gently press the LNDOUBLER 5/8 into the socket. Now inspect the installation of the LNDOUBLER 5/8 making sure that all the pins are seated in the socket. If the LNDOUBLER 5/8 will not seat properly due to obstruction by a component which cannot be repositioned easily,it may be necessary to RAISE the LNDOUBLER 5/8 in its socket. This can be accomplished by installing a 40 pin dip IC socket between the LNDOUBLER 5/8 pins and the IC socket on the expansion interface.

Before closing up, note the switch on the outside corner of the LNDOUBLER 5/8. It is accesible from the outside of the interface, but you must make sure you know what position it is set to before closing up the interface. SET THE SWITCH TO THE "5" POSITION. A detailed explanation of the operation of this switch is included in a later section of this manual.

Reconnect the power supply connector at J1 noting that the correct way to connect J1 is such that the connector "locks" in place. Position the circuit board back in place with the component side down. Reinstall the four circuit board mounting screws. Note that their should be three screws with washers and one without. The one without is the one closest to the RS232 BAUD rate configuration area. Position the case top back on top of the chassis,install the top and bottom support screws.

Observe the opening in the interface that the 5/8 switch is visible. Using some sort of label or tape, mark the outside of the case in such a way as to identify the setting of the switch for the "5" position. Proceed to the section entitled "POWERING UP FOR THE FIRST TIME".

LNW SYSTEM EXPANSION (KIT FORM)

Follow the instructions as for the assembled and test unit but it WILL be necessary to obtain and install a 40 pin dip IC socket as a spacer between the LNDOUBLER 5/8 and the interface socket if sockets were used in any of the IC's surrounding U14.

POWERING UP FOR THE FIRST TIME

CAUTION

DO NOT INSTALL A DOUBLE DENSITY SYSTEM DISK INTO THE DISK DRIVE AT THIS TIME!!! PROPER OPERATION UNDER SINGLE DENSITY MUST BE ESTABLISHED PRIOR TO ATTEMPTING TO BOOT THE DOUBLE DENSITY (DOSPLUS) SYSTEM DISK. INSTALLING YOUR ONLY COPY OF A DOUBLE DENSITY SYSTEM DISK WHEN PROPER INSTALLATION HAS NOT BEEN ESTABLISHED MAY LEAD TO NEEDLESS FRUSTRATION AND DELAY

Reconnect power,your cpu (keyboard),and floppy cable to your interface. Do not connect a printer or RS232 cable until proper operation has been established below.

Power your drives, the interface, and insert the SINGLE DENSITY SYSTEM DISK that you created while testing your interface into your drive Ø.

Turn on the CPU

If the SINGLE DENSITY disk boots correctly, replace the single density system disk with the DOUBLE DENSITY system disk.

Reset the CPU

If the disk boots correctly, proceed to make a backup of the Double density system disk. If it backs up correctly, proceed to reconnect the rest of your peripherals and enjoy the most reliable double density operation possible! If any problems occur, turn the system off and proceed to the section of the manual entitled "TROUBLESHOOTING".

CONNECTING EIGHT INCH DISK DRIVES

Eight inch disk drives which are SHUGART compatible can easily be connected to an expansion interface or SYSTEM EXPANSION with the LNDOUBLER 5/8 installed. A special cable adaptor board which converts the 34 conductor 5.25" floppy cable to the 5Ø conductor 8" drive cable is available from LNW RESEARCH CORPORATION ,stk#1Ø96. One end of the adaptor board plugs into your 5" drive cable (cable with no pins pulled) and the other end of the adaptor plugs into your 8" drive cable, thus interfacing the 8" drive(s) to your system. The adaptor board also has a connection for the "TG43" or write current line which may be needed if your 8" drive requires it. If it is needed , it may be ordered from LNW. The 8" drive , 4-disk cable is also available from LNW. Since all 8" disk drives are not the same compare the following chart with the pinouts for the drive that you plan to be using. The following chart also shows the simularities between the 5" and 8" disk drive interface lines.

PIN # 5"	SIGNAL	PIN # 8"	SIGNAL
		2	ground (write current)
		4	not used
		6	not used
		8	not used
		1Ø	two sided (not used)
		12	disk change (not used)
		14	side select
		16	activity indicator
2	not used	18	head load (not used)
4	not used	2Ø	index
6	not used	22	ready (not used)
8	index	24	not used
1Ø	drive select 1	26	drive select 1
12	drive select 2	28	drive select 2
14	drive select 3	3Ø	drive select 3
16	motor on	32	motor on
18	direction select	34	direction select
2Ø	step	36	step
22	write data	38	write data
24	write gate	4Ø	write gate
26	track Ø	42	track Ø
28	write protect	44	write protect
3Ø	read data	46	read data
32	drive select 4/side select	48	not used
34	not used	5Ø	not used

WAIT STATE CABLE

If you intend to run operating systems other than DOSPLUS 3.38 and NEWDOS80 2.0 with 8" drive support, you may need the special "WAIT CABLE" wired from the "wait pin" on the LNDOUBLER 5/8 to pin 33 of the screen printer bus. This line causes the CPU to wait in order to pick up the data correctly while doing disk I/O. Since improvements have been made in the operating systems as far as the disk I/O is concerned,it has been found that the 1.77mhz cpu speed is adequate to handle the data rate of the 8" disk drive without any special hardware. Hopefully the operating systems which have in the past required this logic, will rewrite their disk I/O routines to eliminate this unnecesary cable. The "WAIT CABLE" IS AVAILABLE from LNW RESEARCH. Order information is included in the rear of this manual.

EIGHT INCH DISK DRIVE OPERATION

If you want to use 8" disk drives, either mixed with 5" drives or only with 8" drives make sure that 5" operation is assured. After connecting the 8" disk drive to your system as described , attempt to format an 8" disk drive. If it formats correctly, flip the 5/8 switch in the rear and boot an 8" system disk, reconfiguring your drives so as to have an 8" drive at drive 0. If it works, set up your drives and the 5/8 switch as you would like and enjoy the increased density and reliability of eight inch disk drives! If problems result, consult the section in the manual entitled"TROUBLESHOOTING".

INSTALLING A SPEED UP KIT IN YOUR TRS80

Changing the speed of the CPU in a TRS80 involves more than just changing the Z80 to a Z80A. It involves soldering,wiring and a comprehensive plan to obtain the correct timing for the 4116 memory components in the INTERFACE as well as in the CPU . The speed up kit required to run 8" double density must be at least twice the standard speed,and MUST NOT return to the slow speed under disk I/O. One such speed up kit is available from :

ARCHBOLD ELECTRONICS
10708 Segovia Way
Rancho Cordova CA 95670

We do not recommend such a speed up kit for someone who does not have a certain degree of technical skill in electronics and is proficient in soldering.

For further details concerning the installation of speed up kits and other modifications to the TRS80 we recommend the following book:

THE CUSTOM TRS80 and other mysteries by Dennis Kitsz
available from- IJG COMPUTER SERVICES
1260 West Foothill blvd
Upland CA 91786

TROUBLESHOOTING

We have included a list of symptoms and possible solutions to aid in the search for your problem. Most common problems occur from hasty late night installations. Try everything imaginable before coming to the conclusion that LNDOUBLER 5/8 is at fault. We will be glad to assist you in problems concerning the installation of the LNDOUBLER 5/8. We cannot help you with custom installations nor can we install your LNDOUBLER 5/8 for you. We cannot help you in determining if your 8" disk drive will work with the LNDOUBLER 5/8 nor can we recommend ways to modify 8" disk drives which are not SHUGART compatible.If you are having problems with configuring your 8" disk drive, contact the manufacturer or dealer that sold the drive.We cannot help you with problems related to your 8" drives unless you are using the cables and cable adaptors which WE manufacture! We will not talk to you about wiring the LNDOUBLER 5/8 to other computers or other interfaces.(ie. MOD III or PMC8Ø)

HERE ARE SOME OF THE COMMON PROBLEMS

SYMPTOM: Single density DOS disk won't boot. Motor turns on, drive light turns on...then turns off.

PROBABLE CAUSE:

1. 5/8 switch set to 8" position
2. Defective single density disk
3. Improper power up procedure, power up again
4. FD1771 improperly installed in LNDOUBLER 5/8
5. Improper installation of the LNDOUBLER 5/8

SYMPTOM: Nothing happens on power up .Computer displays "memory size?" or similar message.

PROBABLE CAUSE:

1. Expansion interface not powered up
2. LNDOUBLER 5/8 improperly installed

SYMPTOM: Single density disk boots but double density operating system disk will not boot or does not function.

PROBABLE CAUSE:

1. Defective double density system disk...Contact your dealer about receiving a new copy.
2. Improper termination of your disk drives.

SYMPTOM: Single and Double density disks boot correctly but will not backup or write to disk in any density.

PROBABLE CAUSE:

1. More than one disk drive with termination resistors installed.Last disk drive on cable should have the termination resistor packs.
2. Improper installation of LNDOUBLER 5/8 (may have a pin on the doubler bent)
3. Defective FD1771 IC

SYMPTOM: Double density operation is correct but will not format, backup or write to disk correctly in single density.

PROBABLE CAUSE:

1. Improper installation of FD1771
2. Defective FD1771

SYMPTOM: 5" single and double density operation is correct,but 8" drives will not function.

PROBABLE CAUSE:

1. Improper configuration of 8" disk drive
2. Improper termination of 8" disk drive
3. 8" disk drive cabling defective
4. Configuration of 8" disk drive wrong

SYMPTOM: 8" disk drive operation in single density is correct but double density 8" will not work.

PROBABLE CAUSE:

1.Attempting to run 8" double density on an unmodified TRS-80 (1.77 mhz CPU speed)
2.Speed up kit forces low cpu speed (1.77mhz) during disk I/O
3.Speed up kit does not bring the CPU up to 3.55 mhz

SYMPTOM: 8" single density will not operate under OMIKRON CP/M or NEWDOS80 1.0.

PROBABLE CAUSE:

1."WAIT CABLE" not installed between LNDOUBLER 5/8 and pin 33 of the screen printer bus.

SYMPTOM: DOSPLUS 3.3 will not boot

PROBABLE CAUSE:

1. The original DOSPLUS 3.3d is NOT compatible with the LNDOUBLER 5/8 in ANY FORM, although DOSPLUS 3.2d is compatible in double density with 5" drives only.Although you cannot boot,or use any of the utilities of the DOSPLUS 3.3d you can copy or transfer all your programs or data from the 3.3 disk to your new 3.38 system disk.

SYMPTOM: Problems occur in double density 8" in the upper tracks.

PROBABLE CAUSE:

1. Above track 43 the write current must be lowered on some 8" disk drives. If the drive you have has a signal called "write current switch" then the "TG43" cable must be installed between the LNDOUBLER 5/8 and the 8" disk adaptor board.

2. Diskettes not rated for double density operation

SYMPTOM: When attempting to write on a 8" disk, the DOS error indicates that the disk is "WRITE PROTECTED".

PROBABLE CAUSE:

1.8" disk drives have the opposite convention for WRITE PROTECT. The write protect tab must be installed IN ORDER TO WRITE ON THE DISK.

RETURNING YOUR LNDOUBLER 5/8 FOR REPAIR

If you cannot get your LNDOUBLER 5/8 to function properly within the warranty period, you may elect to return the LNDOUBLER 5/8 to your dealer for replacement (usually the fastest remedy) or you may return it to the factory for repair(provided you filled out the warranty registration and provide proof of purchase from an authorized dealer of LNW RESEARCH CORPORATION).Give our Service Department a call before returning it so a technician can try and help you over the phone. If the LNDOUBLER 5/8 is out of warranty then call the factory and return the defective unit for repair.Service rates will be given to you over the phone at the time you call.

When returning anything to the factory for repair be sure to:

1. Pack it properly with plenty of padding
2. Ship it prepaid UPS or Insured PARCEL POST
3. Enclose a complete description of the problem
4. Warranty units should include PROOF OF PURCHASE

NOTE

Problems concerning the operation of the operating system diskette supplied with the LNDOUBLER 5/8 as well as its updates should be directed to the authors of the operating system .

THEORY OF OPERATION

The LNDOUBLER 5/8 has as it's heart two floppy controller IC's- the FD1771 (single density controller) and the FD1791 (single and double). The reason that the 1771 is still needed when the 1791 can do single density operation is that the commands are slightly different and the BOOT in the level 2 ROMs would not work. And since we want to stay 100% software compatible we keep the FD1771. The two floppy controller IC's are tied together so only one of the two can be enabled at one time.We turn on the 1771 when we do single density disk I/O and we enable the 1791 for double density operation.

To switch from 5.25" disk drives to 8" inch disk drives we must change the frequency of the clock going into the 1771 and 1791 and do some other switching of signals. A software switch is also provided for this. In addition there exists some special "wait state logic" which allows 8" disk drive operation under a slow CPU speed.This logic is used by several operating systems and is maintained for compatibility reasons.It may also be found that this logic can be used for 8" double density operation with a 1.77mhz cpu speed.

The software switch locations are summarized in the chart below:

ACTION	WRITE TO PORT	WITH DATA
single>>double	37EC (H)	FF (H)
double>>single	37EC	FE
5.25">>8"	37EE	CØ
8">>5.25"	37EE	AØ
wait logic>"on"	37EE	EØ
wait logic>"off"	37EE	CØ

Whenever any switching is done the floppy controller which is NOW enabled is initialized and all the internal registers restored.Refer to the data sheets supplied in the back of this section for programming information concerning the floppy controller IC's.Although the "wait" logic need not be invoked for single density operation for 8" drives at the 1.77mhz CPU speed an explanation of it's operation follows-

1. The wait state logic is turned on
2. The floppy controller is initialized and the registers set
3. The command is given to floppy controller to read or write.
4. The status register is read. This causes the wait state logic to issue a "wait" to the Z8Ø CPU UNTIL:
   a. the busy bit in the status register goes false
   or b. DRQ on the floppy controller chip goes true
   or c. IRQ on the floppy controller chip goes true

If the condition that removed the wait was (a.) or (b.) above then the wait state logic is still "on" but the CPU wait was only removed until the next time the status register of

the floppy controller is read. If the condition that removed the wait was (c.) then the wait state logic is turned "off" .

ANALOG PHASE LOCK LOOP DATA SEPARATION

The VCO -the voltage controlled oscillator a 74LS629 at IC15 generates the 4mhz VCO frequency (2mhz for 5.25" disk drive operation) for the WD1691 the floppy support logic IC(at IC8). In order to guarantee that it is not sensitive to power supply variations from interface to interface,VR1 (78L05) provides a regulated supply to the 74LS629 and the adjustment controls R25 and R26. The 74LS629 is an improved version of the 74S124 providing excellent immunity to temperature variation and aging. R25 is a multiturn pot to adjust the frequency range and R26 adjusts the bias voltage (for a stable "free running" frequency)for the VCO. The WD1691 and the 74LS629 make up the ANALOG PHASE LOCK LOOP DATA SEPARATION.

PRECISION WRITE PRECOMPENSATION

The WD2143 provides an accurate write precompensation value according to the adjustment of R24. A negative true pulse of the actual precompensation value can be observed with an oscilloscope at IC8 pin 4. Write precompensation is factory aligned to 200 ns +-25ns and is enabled only for double density operation (all tracks 5.25" and tracks above 43 for 8"). The interface between the WD 2143 and the WD1691 is explained in some detail in the data sheets supplied. Schematics and further details are beyond the scope of this manual.

5/8 SWITCH

On powerup or reset, the LNDOUBLER 5/8 switches to 5.25" or 8" drive operation depending on the setting of the 5/8 switch. Since the LNDOUBLER 5/8 always powers up in single density for compatibility reasons,the system disk must always have a single density boot at track 0,sector 0. This applys also to double density 8" system disks.Note that data disks are not required to have any single density tracks.

DATA SHEETS

The following data sheets are provided for those interested in the technical details concerning the FD1791,WD1691,and the WD2143.The data sheets have been edited to conserve space and we are not distributing the unedited data sheets.The data sheets are reprinted with the permission of WESTERN DIGITAL CORPORATION. Write precompensation is thoroughly discussed as well as the relative performance of the phase lock loop and the rom programmed counter type data separation design techniques.

For those interested in more details concerning how to program the floppy controller IC's in your computer ,the following book is recommended:

TRS-8Ø MODEL I DISK INTERFACING by
William Barden Jr.
available from - 8Ø-US Journal (2Ø6) 475-2219

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

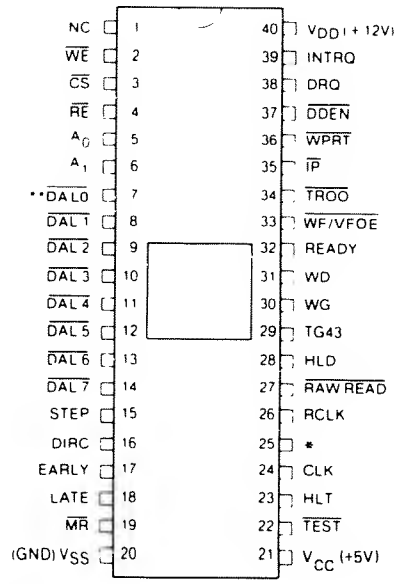
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

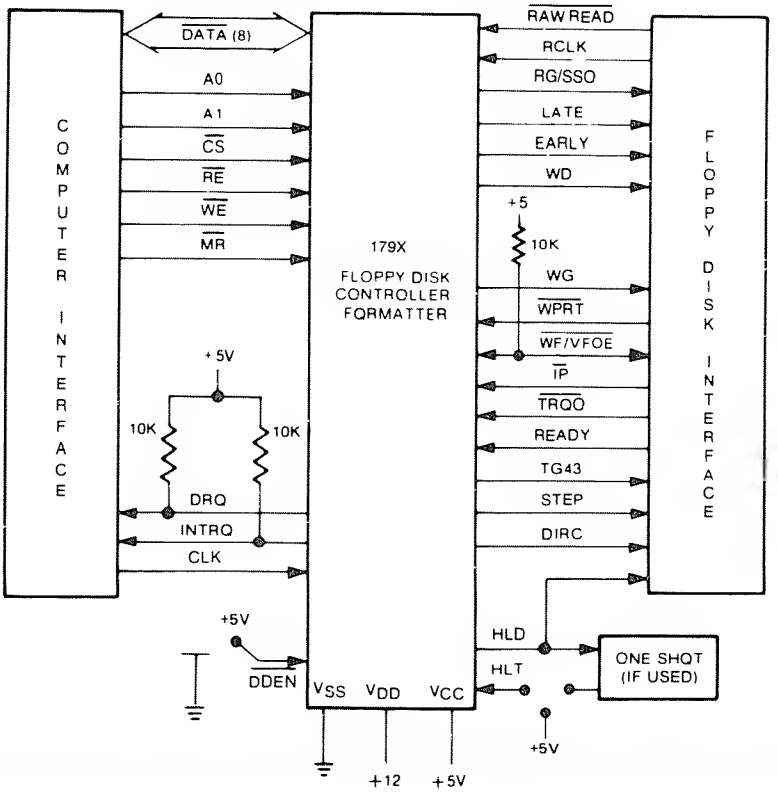
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{\text{MR}}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{\text{MR}}$ ACTIVE. When $\overline{\text{MR}}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{\text{WE}}$	A logic low on this input gates data on the DAL into the selected register when $\overline{\text{CS}}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{\text{CS}}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{\text{RE}}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{\text{CS}}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{\text{RE}}$ and $\overline{\text{WE}}$ control: A1 A0 $\overline{\text{RE}}$ $\overline{\text{WE}}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{\text{DAL0}}$-$\overline{\text{DAL7}}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{\text{WE}}$ or transmitter enabled by $\overline{\text{RE}}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ / VFO ENABLE	$\overline{\text{WF}}$/$\overline{\text{VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

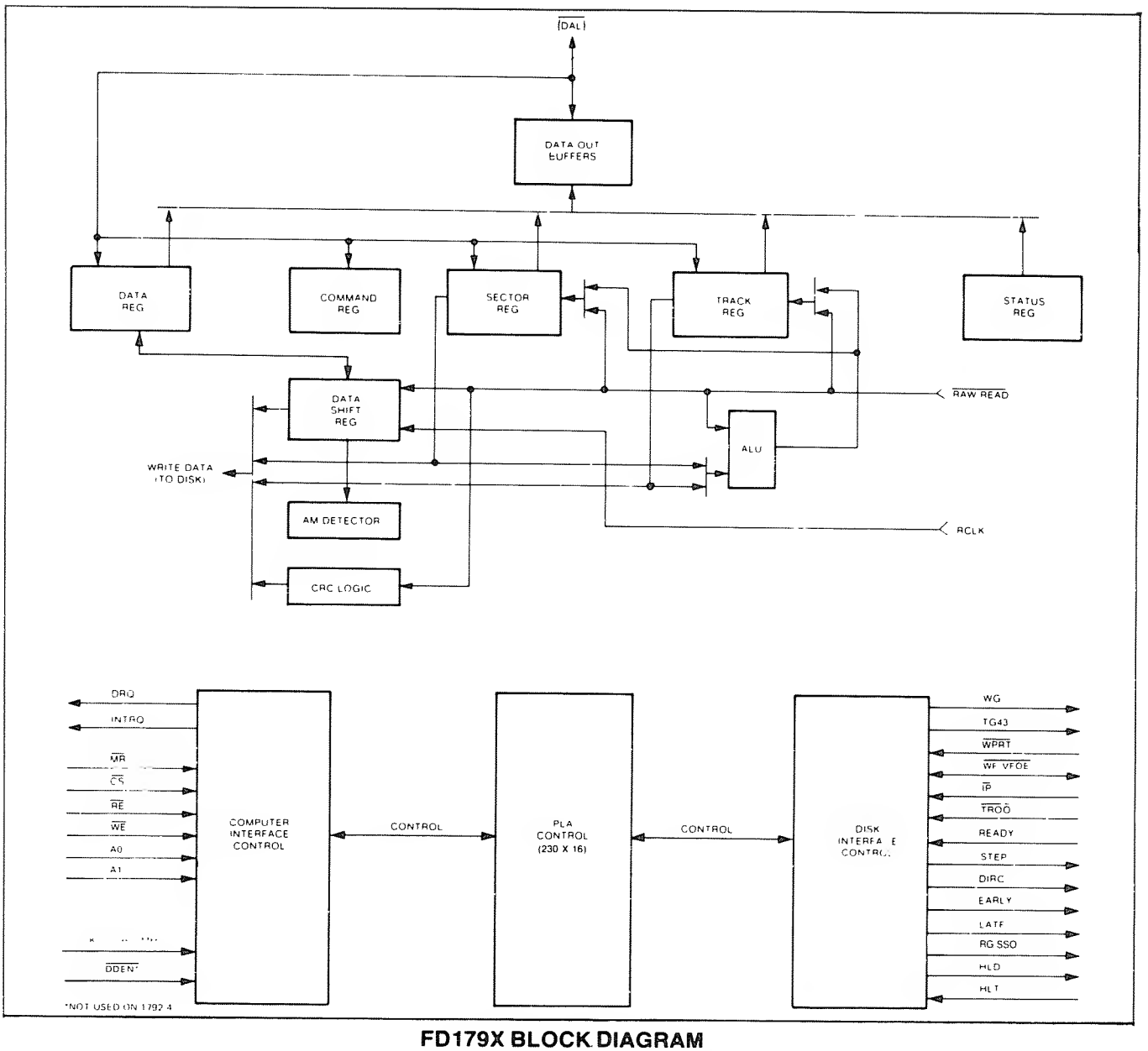
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

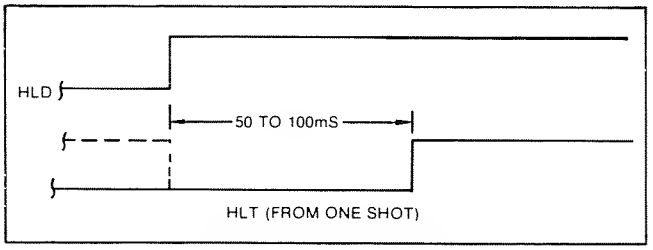
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the $\overline{\text{Write Fault}}$ bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)
- h = 1, Load head at beginning
- h = 0, Unload head at beginning

V = Verify flag (Bit 2)
- V = 1, Verify on destination track
- V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)
- u = 1, Update Track register
- u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)
- m = 0, Single Record
- m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)
- a_0 = 0, FB (Data Mark)
- a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)
- E = 1, 15 ms delay
- E = 0, no 15 ms delay

(F_2) S = Side Select Flag (1791/3 only)
- S = 0, Compare for Side 0
- S = 1, Compare for Side 1

(F_1) C = Side Compare Flag (1791/3 only)
- C = 0, disable side select compare
- C = 1, enable side select compare

(F_1) S = Side Select Flag

(Bit 1, 1795/7 only)
- S = 0 Update SSO to 0
- S = 1 Update SSO to 1

(F_2) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)
- I0 = 1, Not-Ready to Ready Transition
- I1 = 1, Ready to Not-Ready Transition
- I2 = 1, Index Pulse
- I3 = 1, Immediate Interrupt

I_3 -I_0 = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

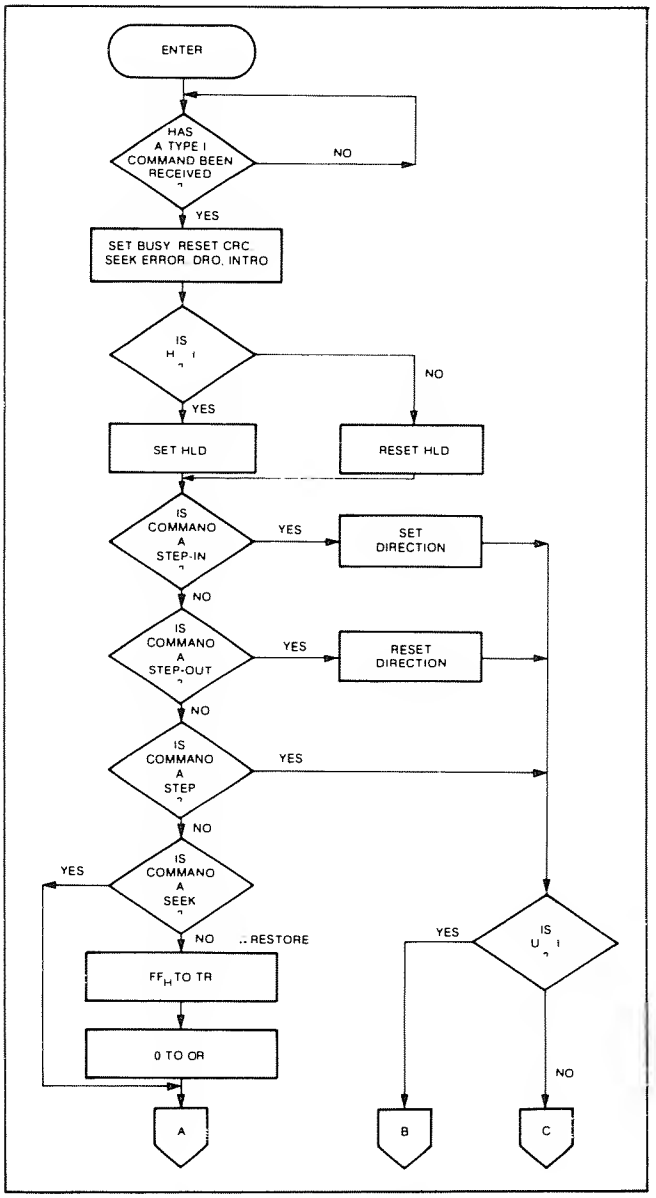
The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

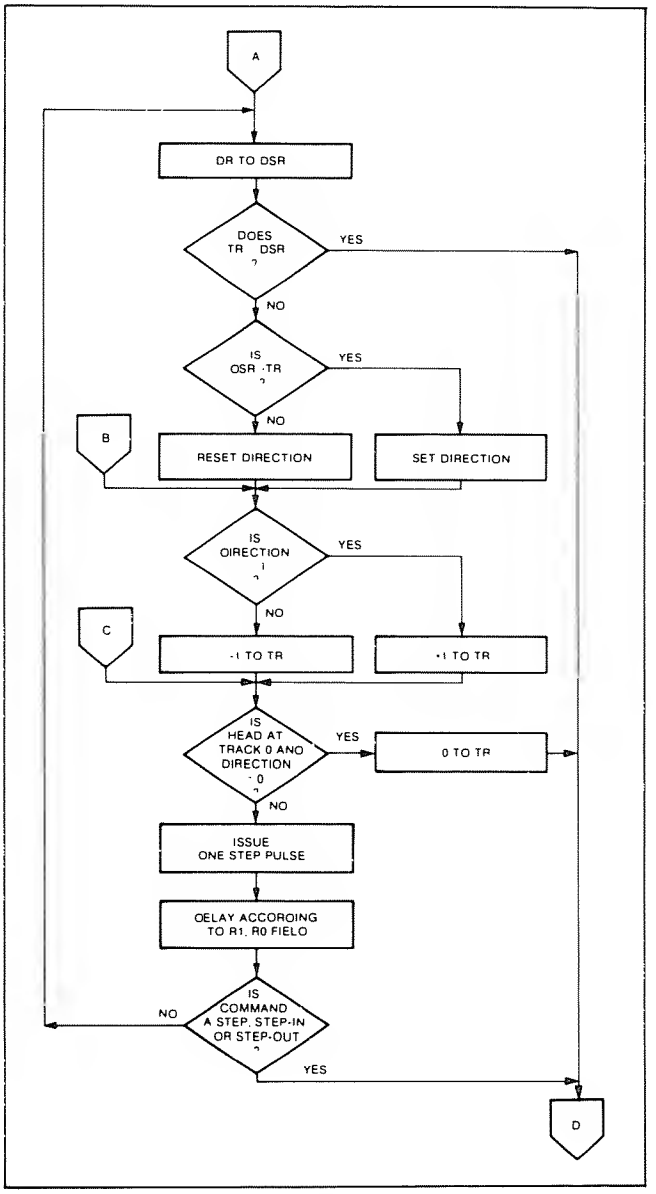
During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



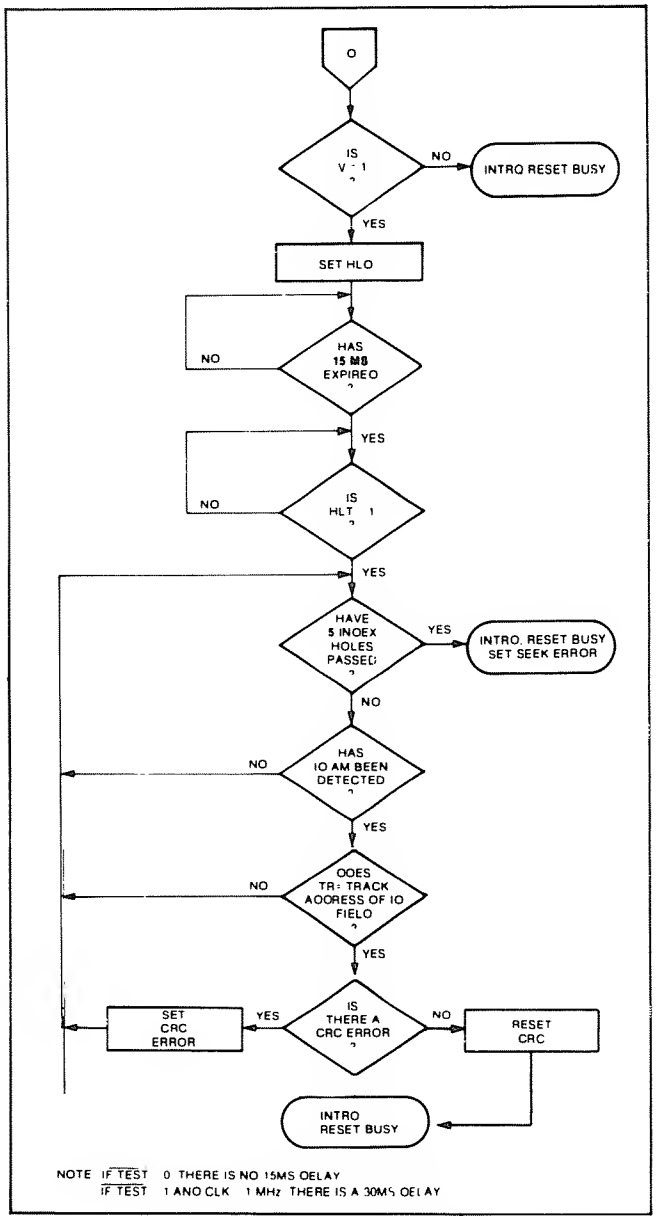
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r1r10 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

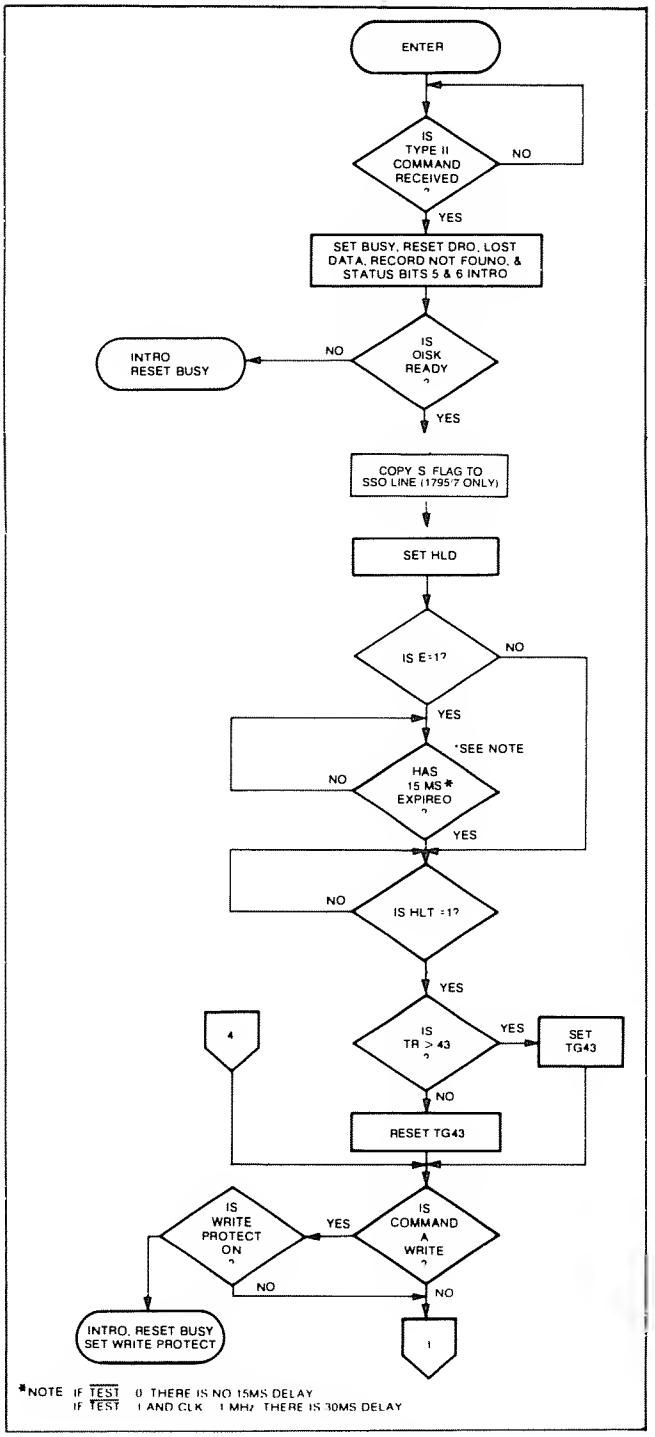
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-

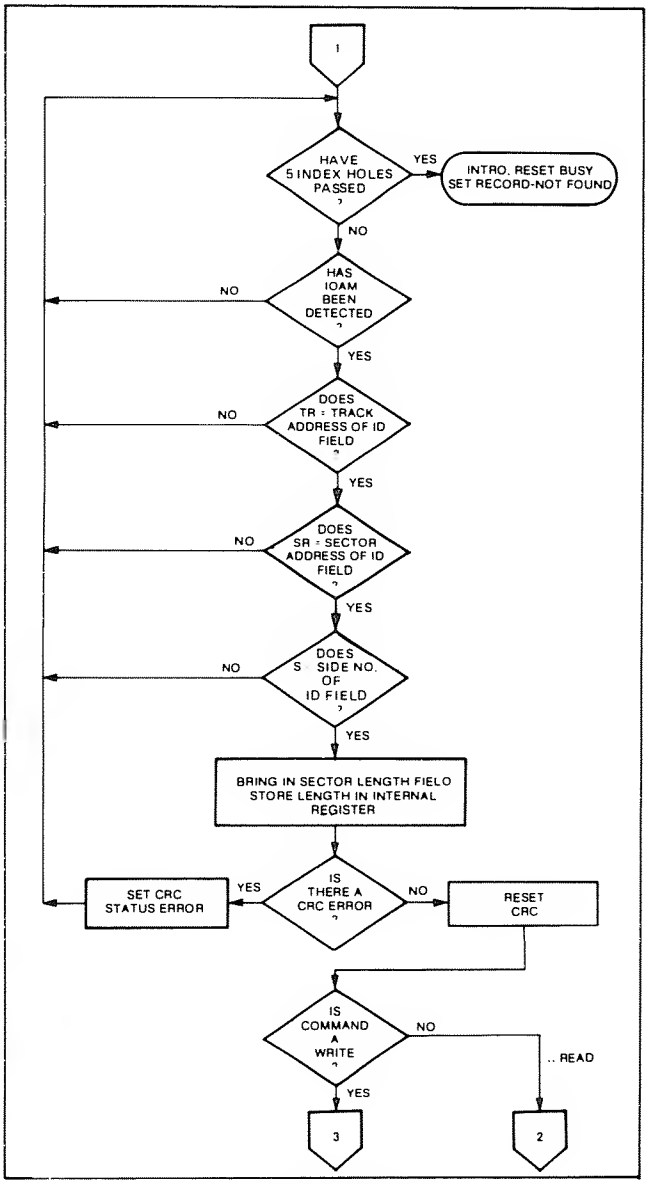
countered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-



TYPE II COMMAND



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

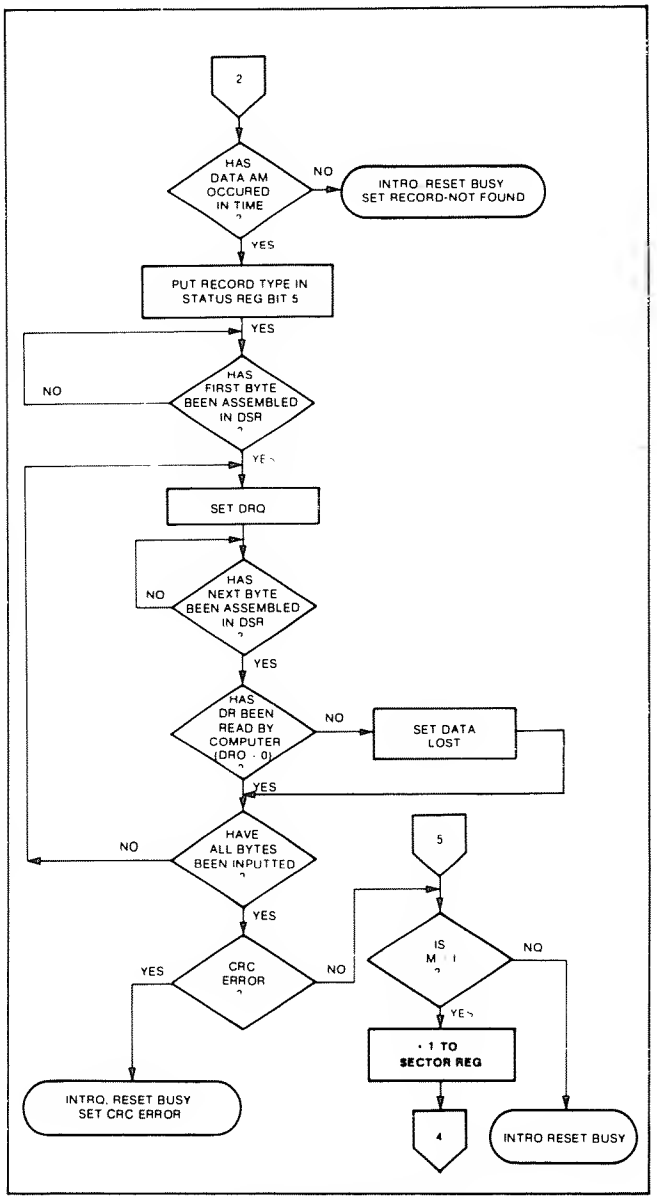
The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

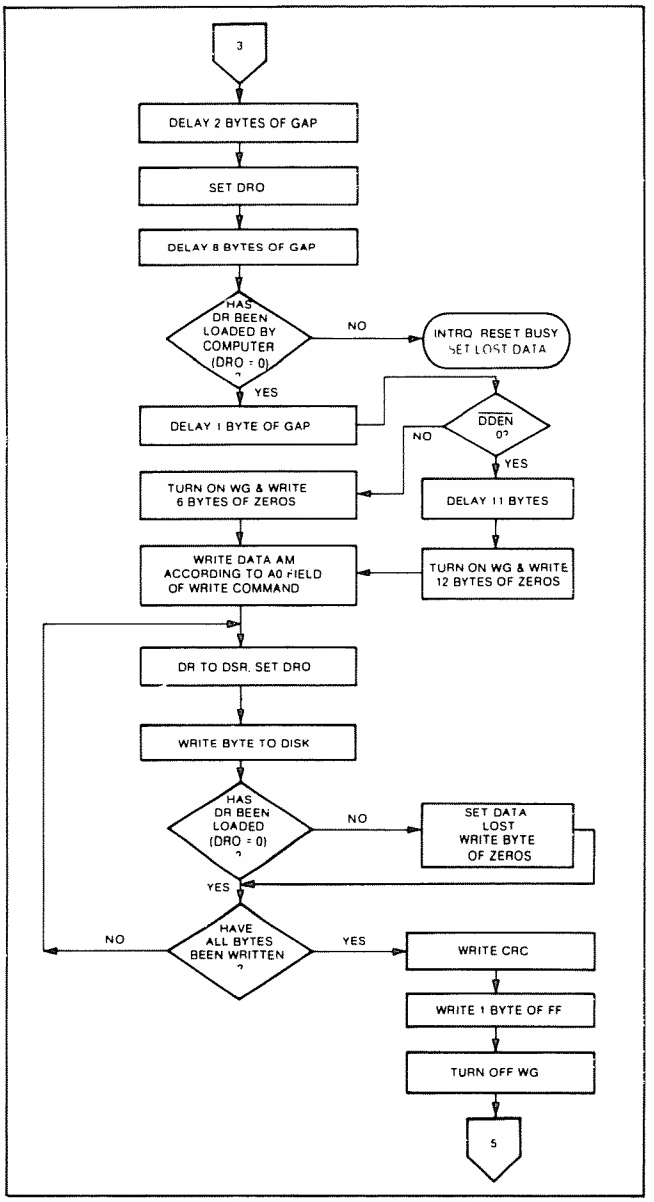
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

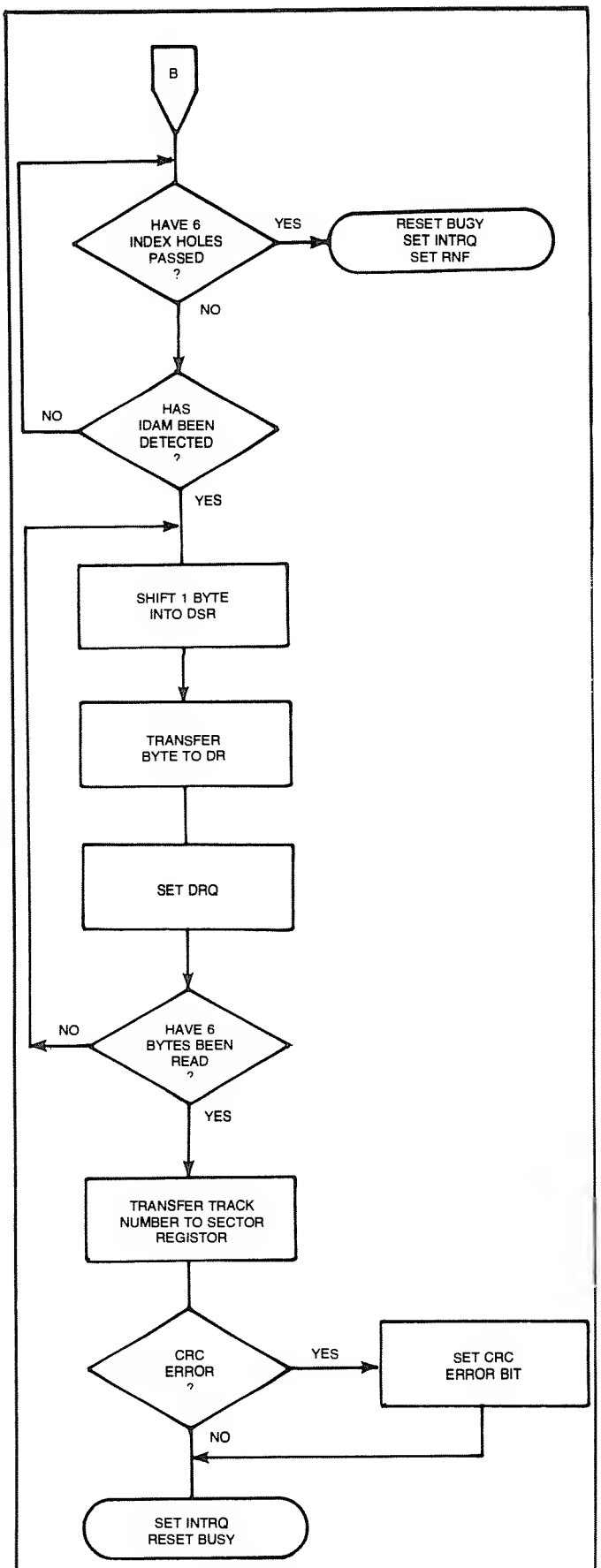
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE III COMMAND

Read Track/Address

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. *This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.*

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TROO}}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

October, 1980

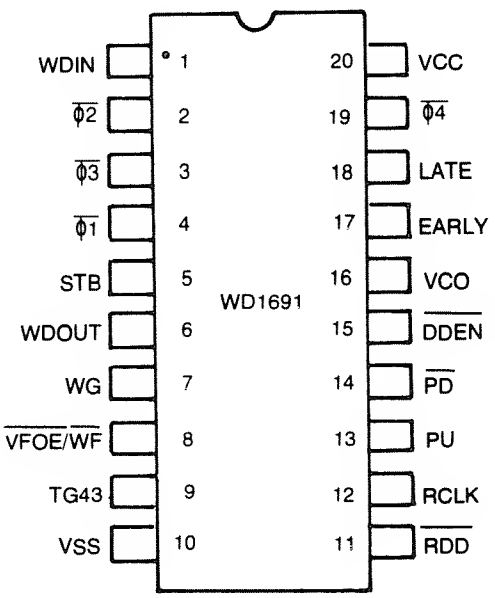
FEATURES

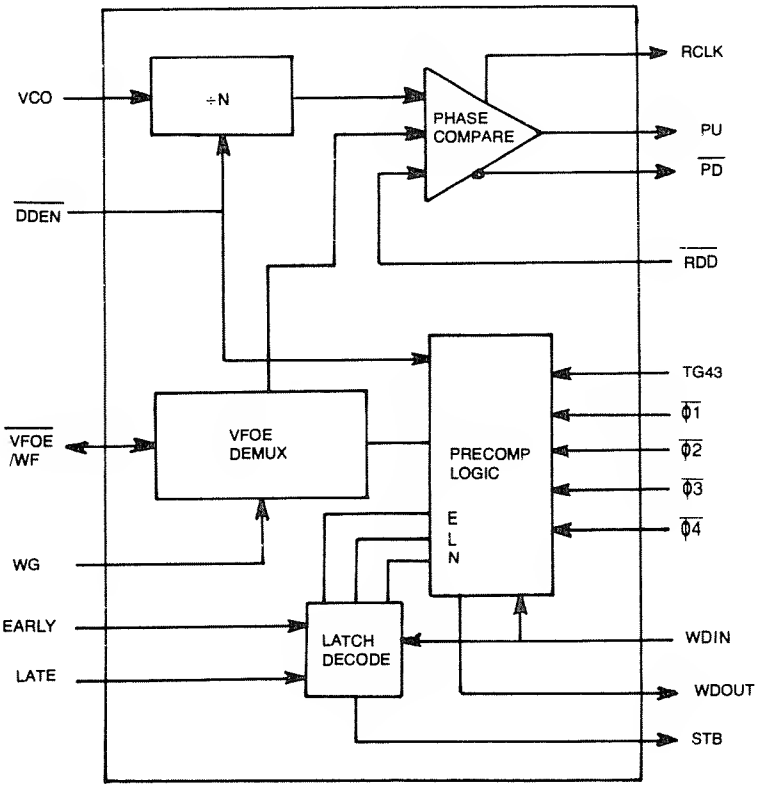
- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- VFOE/WF Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.





BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4,19	PHASE 2, 3, 1, 4	$\overline{\Phi 2}$ $\overline{\Phi 3}$ $\overline{\Phi 1}$ $\overline{\Phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	$\overline{VFOE}/\overline{WF}$	Ties directly to the FD179X $\overline{VFOE}/\overline{WF}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
10	V_{ss}	V_{ss}	Ground
11	READ DATA	$\overline{RDD}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{PD}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{DDEN}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{cc}	V_{cc}	+ 5V ± 10% power supply

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: DDEN, VCO, RDD, and VFOE/WF; and three outputs: PU, PD and RCLK. The VFOE/WF input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When VFOE/WF and WRITE GATE are low, the data recovery circuit is enabled. When the RDD line goes Active Low, the PU or PD signals will become active. If the RDD line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an *increase* in VCO frequency. If the RDD line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 (DDEN=1) or a divide-by-8 (DDEN=0) of the VCO frequency.

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case, $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, $\overline{\phi 4}$, and STB should be tied together, DDEN left open, and TG43 tied to ground.

In the double-density mode ($\overline{DDEN}$=0), the signals Early and Late are used to select a phase input ($\overline{\phi 1}$ – $\overline{\phi 4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation. $\overline{\phi 2}$ is used as the write data pulse on nominal (Early=Late=$\overline{\phi}$), $\overline{\phi 2}$ is used for early, and $\overline{\phi 3}$ is used for late. The leading edge of $\overline{\phi 4}$ resets the STB line in anticipation of the next write data pulse. When TG43=0 or DDEN=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while $\overline{DDEN}$=0.

The signals, $\overline{DDEN}$, TG43, and $\overline{RDD}$ have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of ± 1V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and $\overline{PD}$ signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or $\overline{PD}$ signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns. (VCO = 4MHz, DDEN = 0) or 500ns. (VCO = 4MHz, DDEN = 1), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, and ideal condition for the FD179X internal recovery circuits.

FD179X Application Notes

JUNE, 1980

INTRODUCTION

Over the past several years, the Floppy Disk Drive has become the most popular on-line storage device for mini and microcomputer systems. Its fast access time, reliability and low cost-per-bit ratio enables the Floppy Disk Drive to be *the* solution in mass storage for microprocessor systems. The drive interface to the Host system is standardized, allowing the OEM to substitute one drive for another with minimum hardware/ software modifications.

Since Floppy Disk Data is stored and retrieved as a self-clocking serial data stream, some means of separating the clock from the data and assembling this data in parallel form must be accomplished. Data is stored on individual Tracks of the media, requiring control of a stepper motor to move the Read/Write head to a predetermined Track. Byte sychronization must also be accomplished to insure that the parallel data is properly assembled. After all the design considerations are met, the final controller can consist of 40 or more TTL packages.

To alleviate the burden of Floppy Disk Controller design, Western Digital has developed a Family of LSI Floppy Disk controller devices. Through its own set of macro commands, the FD179X Controller Family will perform all the functions necessary to read and write data to the drive. Both the 8" standard and 5¼" mini-floppy are supported with single or double density recording techniques. The FD179X is compatible with the IBM 3740 (FM) data format, or the System 34 (MFM) standards. Provisions for non-standard formats and variable sector lengths have been included to provide more storage capability per track. Requiring standard +5, +12 power supplies the FD179X is available in a standard 40 pin dual-in-line package.

The FD179X Family consists of 6 devices. The differences between these devices is summarized in Figure 1. The 1792 and 1794 are "single density only" devices, with the Double Density Enable pin (DDEN) left open by the user. Both True and inverted Data bus devices are available. Since the 179X can only drive one TTL Load, a true data bus system may use the 1791 with external inverting buffers to arrive at a true bus scheme. The 1795 and 1797 are identical to the 1791 and 1793, except a side select output has been added that is controlled through the Command Register.

SYSTEM DESIGN

The first consideration in Floppy Disk Design is to determine which type of drive to use. The choice ranges from single-density single sided mini-floppy to the 8" double-density double-sided drive. Figure 2 illustrates the various drive and data capacities associated with each type. Although the 8" double-density drive offers twice as much storage, a more complex data separator and the addition of Write Precompensation circuits are mandatory for reliable data transfers. Whether to go with 8" double-density or not is dependent upon PC board space and the additional circuitry needed to accurately recover data with extreme bit shifts. The byte transfer time defines the nominal time required to transfer one byte of data from the drive. If the CPU used cannot service a byte in this time, then a DMA scheme will probably be required. The 179X also needs a few microseconds for overhead, which is subtracted from the transfer time. Figure 3 shows the actual service times that the CPU must provide on a byte-by-byte basis. If these times are not met, bytes of data will be lost during a read or write operation. For each byte transferred, the 179X generates a DRQ (Data Request) signal on Pin 38. A bit is provided in the status register which is also set upon receipt of a byte from the Disk. The user has the option of reading the status register through program control or using the DRQ Line with DMA or interrupt schemes. When the data register is read, both the status register DRQ bit and the DRQ Line are automatically reset. The next full byte will again set the DRQ and the process continues until the sector(s) are read. The Write operation works exactly the same way, except a WRITE to the Data Register causes a reset of both DRQ's.

RECORDING FORMATS

The FD179X accepts data from the disk in a Frequency-Modulated (FM) or Modified-Frequency-Modulated (MFM) Format. Shown in Figures 4A and 4B are both these Formats when writing a Hexidecimal byte of 'D2'. In the FM mode, the 8 bits of data are broken up into "bit cells." Each bit cell begins with a clock pulse and the center of the bit cell defines the data. If the data bit = 0, no pulse is written; if the data = 1, a pulse is written in the center of the cell. For the 8" drive, each clock is written 4 microseconds apart.

FIGURE 1. DEVICE CHARACTERISTICS

DEVICE	SNGL DENSITY	DBLE DENSITY	INVERTED BUS	TRUE BUS	DOUBLE-SIDED
1791	X	X	X		
1792	X		X		
1793	X	X		X	
1794	X			X	
1795	X	X	X		X
1797	X	X		X	X

FIGURE 2. STORAGE CAPACITIES

SIZE	DENSITY	SIDES	UNFORMATTED CAPACITY (NOMINAL)		BYTE TRANSFER TIME	FORMATTED CAPACITY	
			PER TRACK	PER DISK		PER TRACK	PER DISK
5¼"	SINGLE	1	3125	109,375*	64μs	2304**	80,640
5¼"	DOUBLE	1	6250	218,750	32μs	4608***	161,280
5¼"	SINGLE	2	3125	218,750	64μs	2304	161,280
5¼"	DOUBLE	2	6250	437,500	32μs	4608	322,560
8"	SINGLE	1	5208	401,016	32μs	3328	256,256
8"	DOUBLE	1	10,416	802,032	16μs	6656	512,512
8"	SINGLE	2	5208	802,032	32μs	3328	512,512
8"	DOUBLE	2	10,416	1,604,064	16μs	6656	1,025,024

*Based on 35 Tracks/Side
**Based on 18 Sectors/Track (128 byte/sec)
***Based on 18 Sectors/Track (256 bytes/sec)

In the MFM mode, clocks are decoded into the data stream. The byte is again broken up into bit cells, with the data bit written in the center of the bit cell if data = 1. Clocks are only written if both surrounding data bits are zero. Figure 4B shows that this occurs only once between Bit cell 4 and 5. Using this encoding scheme, pulses can occur 2, 3 or 4 microseconds apart. The bit cell time is now 2 microseconds; twice as much data can be recorded without increasing the Frequency rate due to this encoding scheme.

The 179X was designed to be compatible with the IBM 3740 (FM) and System 34 (MFM) Formats. Although most users do not have a need for data exchange with IBM mainframes, taking advantage of these well studied formats will insure a high degree of system performance. The 179X will allow a change in gap fields and sector lengths to increase usable storage capacity, but variations away from these standards is not recommended. Both IBM standards are soft-sector format. Because of the wide variation in address marks, the 179X can only support soft-sectored media. Hard sectored diskettes have continued to lose popularity, mainly due to the unavailability of a standard and the limitation of sector lengths imposed by the physical sector holes in the diskette.

PROCESSOR INTERFACE

The Interface of the 179X to the CPU consists of an 8-bit Bi-directional bus, read/write controls and optional interrupt lines. By selecting the device via the CHIP SELECT Line, each of the five internal registers can be accessed.

Shown below are the registers and their addresses:

PIN 3 CS	PIN 6 A_1	PIN 5 A_0	PIN 4 $\overline{RE}=\emptyset$	PIN 2 $\overline{WE}=\emptyset$
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	H1-Z	H1-Z

Each time a command is issued to the 179X, the Busy bit is set and the INTRQ (Interrupt Request) Line is reset. The user has the option of checking the busy bit or use the INTRQ Line to denote command completion. The Busy bit will be reset whenever the 179X is idle and awaiting a new command. The INTRQ Line, once set, can only be reset by a READ of the status register or issuing a new command. The MR (Master Reset) Line does not affect INTRQ.

The A_0, A_1, Lines used for register selections can be configured at the CPU in a variety of ways. These lines may actually tie to CPU address lines, in which case the 179X will be memory-mapped and addressed like RAM. They may also be used under Program Control by tying to a port device such as the 8255, 6820, etc. As a diagnostic tool when checking out the CPU interface, the Track and Sector registers should respond like "RAM" when the 179X is idle (Busy = INTRQ = 0).

Because of internal synchronization cycles, certain time delays must be introduced when operating under Programmed I/O. The worst case delays are:

OPERATION	NEXT OPERATION	DELAY REQ'D
WRITE TO COMMAND REG	READ STATUS REGISTER	MFM = 14μs* FM = 28μs.
WRITE TO ANY REGISTER	READ FROM A DIFFERENT REG	NO DELAY

*NOTE: Times Double when CLK = 1MHz (5¼" drive)

Other CPU interface lines are CLK, $\overline{MR}$ and $\overline{DDEN}$. The CLK line should be 2MHz (8" drive) or 1MHz (5¼" drive) with a 50% duty cycle. Accuracy should be ±1% (crystal source) since all internal timing, including stepping rates, are based upon this clock.

The $\overline{MR}$ or Master Reset Line should be strobed a minimum of 50 microseconds upon each power-on condition. This line clears and initializes all internal registers and issues a restore command (Hex '03') on the rising edge. A quicker stepping rate can be written to the command register after a $\overline{MR}$, in which case the remaining steps will occur at the faster programmed rate. The 179X will issue a maximum of 255 stepping pulses in an attempt to expect the $\overline{TROO}$ line to go active low. This line should be connected to the drive's $\overline{TROO}$ sensor.

The $\overline{DDEN}$ line causes selection of either single density ($\overline{DDEN}$ = 1) or double density operation. $\overline{DDEN}$ should not be switched during a read or write operation.

FLOPPY DISK INTERFACE

The Floppy Disk Interface can be divided into three sections: Motor Control, Write Signals and Read Signals. All of these lines are capable of driving one TTL load and not compatible for direct connection to the drive. Most drives require an open-collector TTL interface with high current drive capability. This must be done on all outputs from the 179X. Inputs to the 179X may be buffered or tied to the Drives outputs, providing the appropriate resistor termination networks are used. Undershoot should not exceed −0.3 volts, while integrity of V_{IH} and V_{OH} levels should be kept within spec.

MOTOR CONTROL

Motor Control is accomplished by the STEP and DIRC Lines. The STEP Line issues stepping pulses with a period defined by the rate field in all Type I commands. The DIRC Line defines the direction of steps (DIRC = 1 STEP IN/DIRC = 0 STEP OUT).

Other Control Lines include the $\overline{IP}$ or Index Pulse. This Line is tied to the drives' Index L.E.D. *sensor* and makes an active transition for each revolution of the diskette. The $\overline{TROO}$ Line is another L.E.D. sensor that informs the 179X that the stepper motor is at its furthest position, over Track 00. The READY Line can be used for a number of functions, such as sensing "door open", Drive motor on, etc. Most drives provide a programmable READY Signal selected by option jumpers on the drive. The 179X will look at the ready signal prior to executing READ/WRITE commands. READY is *not* inspected during any Type I commands. All Type I commands will execute regardless of the Logic Level on this Line.

WRITE SIGNALS

Writing of data is accomplished by the use of the WD, WG, WF, TG43, EARLY and LATE Lines. The WG or Write Gate Line is used to enable write current at the drive's R/W head. It is made active prior to writing data on the disk. The WF or WRITE FAULT Line is used to inform the 179X of a failure in drive electronics. This signal is multiplexed with the VFOE Line and must be logically separated if required.

The TG43 or "TRACK GREATER than 43" Line is used to decrease the Write current on the inner tracks, where bit densities are the highest. If not required on the drive, TG43 may be left open.

WRITE PRECOMPENSATION

The 179X provides three signals for double density Write Precompensation use. These signals are WRITE DATA, EARLY and LATE. When using single density drives (eighter 8" or 5¼"), Write Precompensation is not necessary and the WRITE DATA line is generally TTL Buffered and sent directly to the drive. In this mode, EARLY and LATE are left open.

For double density use, Write Precompensation is a function of the drive. Some manufacturers recommend Precompensating the 5¼" drive, while others do not. With the 8" drive, Precompensation may be specified from TRACK 43 on, or in most cases, all TRACKS. If the recommended Precompensation is not specified, check with the manufacturer for the proper configuration required.

The amount of Precompensation time also varies. A typical value will usually be specified from 100-300ns. Regardless of the parameters used, Write Precompensation must be done external to the 179X. When $\overline{DDEN}$ is tied low, EARLY or LATE will be activated at least 125ns. before and after the Write Data pulse. An Algorithm internal the 179X decides whether to raise EARLY or LATE, depending upon the previous bit pattern sent. As an example, suppose the recommended Precomp value has been specified at 150ns. The following action should be taken:

EARLY	LATE	ACTION TAKEN
0	0	delay WD by 150ns (nominal)
0	1	delay WD by 300ns (2X value)
1	0	do not delay WD

DATA SEPARATION

The 179X has two inputs (RAW READ & RCLK) and one output (VFOE) for use by an external data separator. The RAW READ input must present clock and data pulses to the 179X, while the RCLK input provides a "window" or strobe signal to clock each RAW READ pulse into the device. An ideal Data Separator would have the leading edge of the RAW READ pulse occur in the exact center of the RCLK strobe.

Motor Speed Variation, Bit shifts and read amplifier recovery circuits all cause the RAW READ pulses to drift away from their nominal positions. As this occurs, the RAW READ pulses will shift left or right with respect to RCLK. Eventually, a pulse will make its transition outside of its RCLK window, causing either a CRC error or a Record-not-Found error at the 179X.

A Phase-Lock-Loop circuit is one method of achieving synchronization between the RCLK and RAW READ signals. As RAW READ pulses are fed to the PLL, minor adjustments of the free-running RCLK frequency can be made. If pulses are occurring too far apart, the RCLK frequency is *decreased* to keep synchronization. If pulses begin to occur closer together, RCLK is *increased* until this new higher frequency is achieved. In normal read operations, RCLK will be constantly adjusted in an attempt to match the incoming RAW READ frequency.

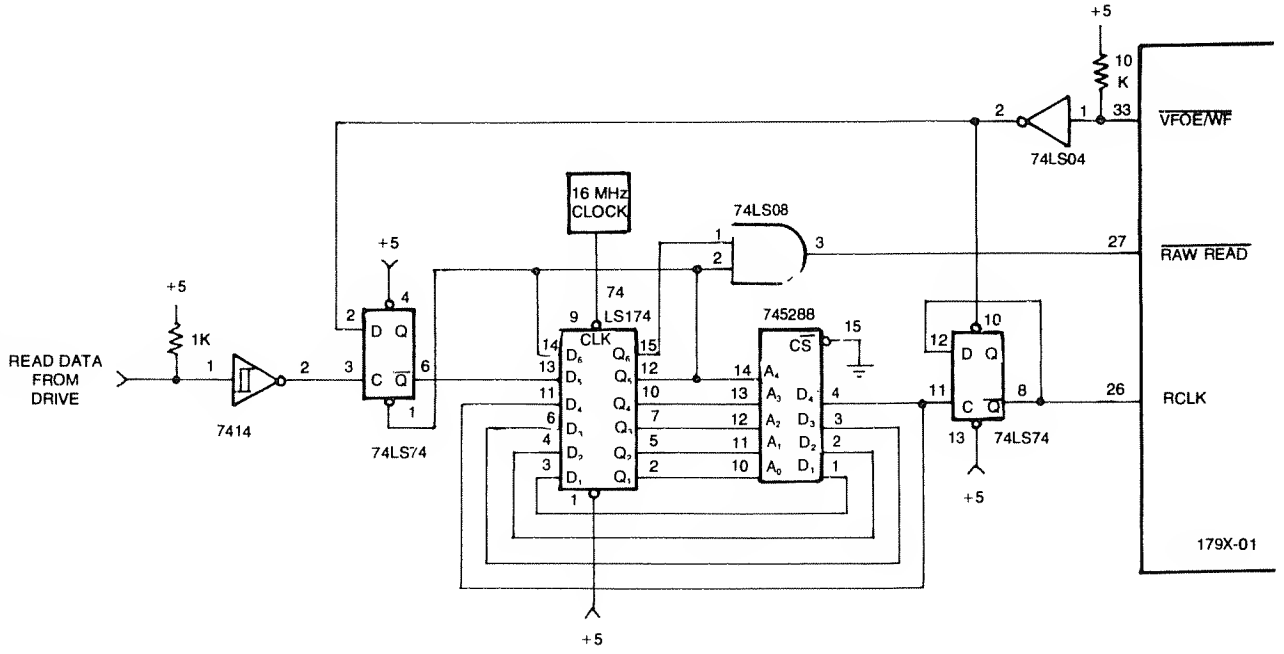
Another method of Data Separation is the Counter-Separator technique. The RCLK signal is again free-running at a nominal rate, until a RAW READ pulse occurs. The Separator then denotes the position of the pulse with respect to RCLK (by the counter value), and counts down to increase or decrease the current RCLK window. The next RCLK window will occur at a nominal rate and will continue to run at this frequency until another RAW READ pulse adjusts RCLK, but only the present window is adjusted.

Both PPL and Counter/Separator are acceptable methods of Data Separation. The PPL has the highest reliability because of its "tracking" capability and is recommended for 8" double density designs.

Figure 12 illustrates a Counter/Separator utilizing a PROM as the count generator. Depending upon the RAW READ phase relationship to RCLK, the PROM is addressed and its data output is used as the counter value. A 16MHz clock is required for 8" double density, while an 8MHz clock can be used for single density.

745288 PROGRAMMING TABLE

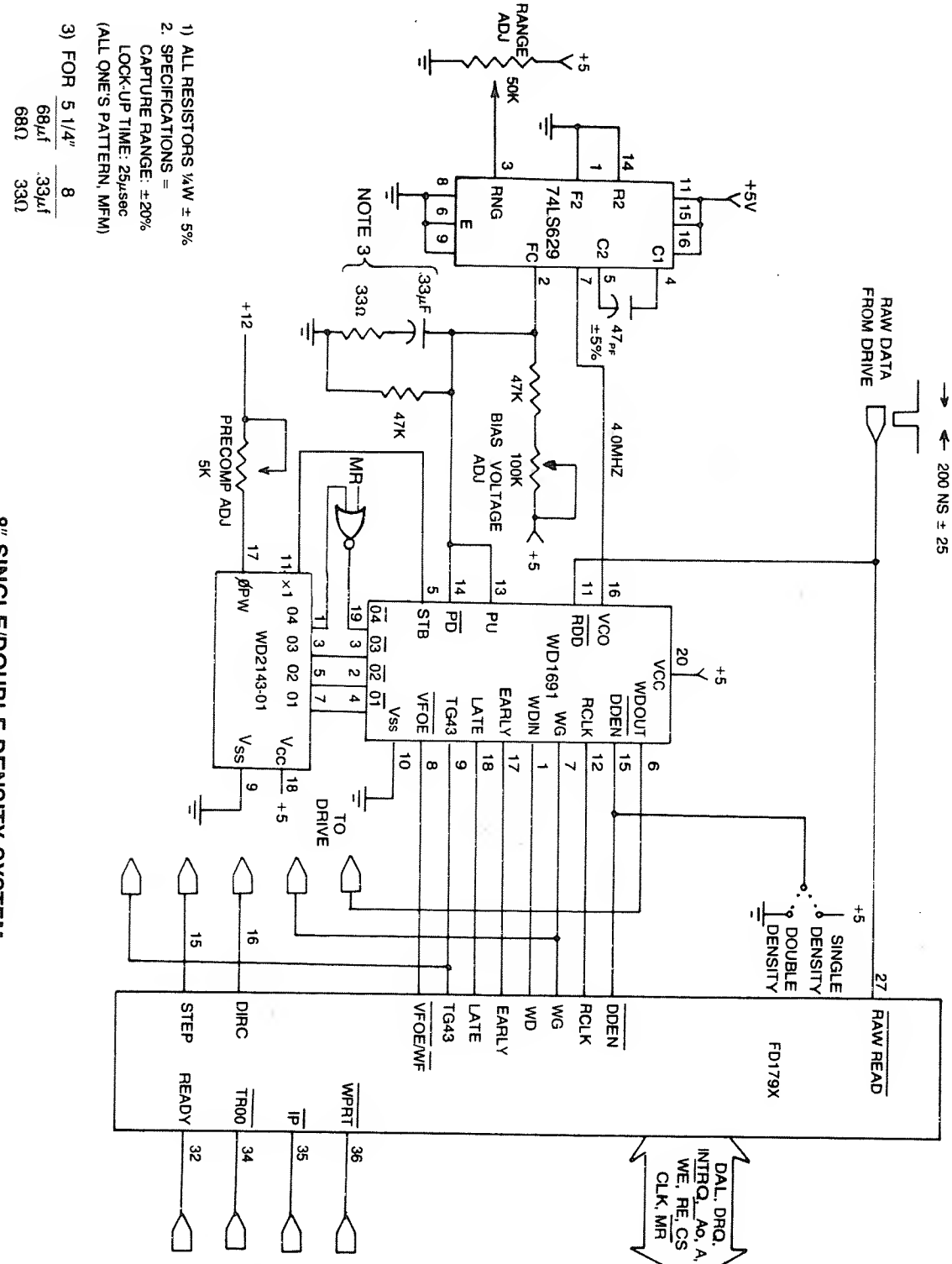
ADDRESS	DATA	ACTION TAKEN
00	01	NONE
01	01	RETARD BY 1 COUNT
02	02	
03	03	
04	03	RETARD BY 2 COUNTS
05	04	
06	05	
07	06	
08	0B	ADVANCE BY 2 COUNTS
09	0D	
0A	0C	
0B	0E	
0C	0F	
0D	0F	ADVANCE BY 1 COUNT
0E	00	
0F	01	
10	01	FREE RUN
11	02	
12	03	
13	04	
14	05	
15	06	
16	07	
17	08	
18	09	
19	0A	
1A	0B	
1B	0C	
1C	0D	
1D	0E	
1E	0F	
1F	00	



179X DATA SEPARATOR

(PROVIDED COURTESY OF ANDROMEDA SYSTEMS, PANDRAMA CITY. CA 91402)

Figure 14 illustrates a PPL data recovery circuit using the Western Digital 1691 Floppy Support device. Both data recovery and Write Precomp Logic is contained within the 1691, allowing low chip count and PLL reliability. The 74S124 supplies the free-running VCO output. The PUMP UP and PUMP DOWN signals from the 1691 are used to control the 74S124's frequency.



1) ALL RESISTORS ¼W ± 5%
2. SPECIFICATIONS =
CAPTURE RANGE: ±20%
LOCK-UP TIME: 25μsec
(ALL ONE'S PATTERN, MFM)

3) FOR 5 1/4" 8"
68μf .33μf
68Ω 33Ω

8" SINGLE/DOUBLE DENSITY SYSTEM

ALIGNMENT

CAUTION

DO NOT ATTEMPT ALIGNMENT ON AN LNDOUBLER 5/8 WHICH IS UNDER WARRANTY AND APPEARS NOT TO FUNCTION AFTER IT WAS FIRST INSTALLED.

ATEMPTING ALIGNMENT ON A LNDOUBLER 5/8 WILL VOID YOUR 180 DAY LIMITED WARRANTY

Alignmnent should not be necessary for the life of the LNDOUBLER 5/8 unless the controls have been tampered with (voids warranty) or ONE of the following parts have been replaced:

VR1,IC15,IC3,IC8,R25,R26,R18,R13,R1,R24,C10

The LNDOUBLER 5/8 may be returned to the factory for alignment if required. Contact the Service Department for the cost of alignment.For those who have the equipment and the "knowhow" to do alignment, the following procedure should only be done in the event that returning the LNDOUBLER 5/8 is a problem AND the LNDOUBLER 5/8 NEEDS ALIGNMNENT!

Equipment Required:
Digital voltmeter 1% accuracy >1megohm input impedance
Frequency counter .1% accuracy >1k ohm input >5mhz
Oscilloscope >15mhz bandwidth ,triggered

DO NOT ATTEMPT ALIGNMENT IF YOU DO NOT HAVE ALL THE EQUIPMENT LISTED ABOVE !

1. Preset the controls and switch settings:
   a. R26- fully counterclockwise
   b. R24- fully clockwise
   c. SW1-"5" position
   d. R25- does not matter

2. Install the LNDOUBLER 5/8 into the expansion interface and apply power to the interface.

3. Adjust R26 for 1.40 VOLTS at IC8 pin 13

4. Adjust R25 for a FREQUENCY measurement of 4.00 Mhz at IC 15 pin 7

5. Boot a disk and set up to format a DOUBLE DENSITY disk. While the it is writing to the disk, measure with the oscilloscope a negative true pulse at IC 8 pin 4. Adjust R24 for a pulse width of 200 ns. This value corresponds to the amount of write precompensation.

ACCESSORY ORDERING INFORMATION

The following accessories may be ordered directly from LNW RESEARCH or your computer dealer.

STOCK NUMBER	DESCRIPTION
1Ø95	LNDOUBLER 5/8
1Ø96	8" cable adaptor circuit board
1Ø97	Wait cable
1Ø98	TG43 cable
1Ø99	8" disk drive cable (4 drive)

In addition to the above products, LNW RESEARCH carries a line of 5" and 8" disk drives and accessories.Call us on price and delivery.

Contact an authorized dealer of LNW RESEARCH or:

LNW RESEARCH CORPORATION
2620 WALNUT AVE.
TUSTIN CA. 92680
(714) 544-5744

For technical info call:
(714) 641-8850

LIMITED WARRANTY

LNW RESEARCH CORPORATION warrants the LNDOUBLER 5/8 to be free from defects in material and workmanship for a period of 18Ø days from the date of delivery- provided the enclosed warranty registration has been completed and returned to LNW RESEARCH CORPORATION within 1Ø days of purchase.This warranty is only valid for ORIGINAL PURCHASERS ONLY and ONLY if the LNDOUBLER 5/8 was purchased from LNW RESEARCH CORPORATION or an AUTHORIZED DEALER of LNW RESEARCH CORPORATION.During the warranty period,the LNDOUBLER 5/8 may be returned to the address below (shipping prepaid) along with PROOF OF PURCHASE for repair, alignment, replacement, or refund at the sole election and expense of LNW RESEARCH CORPORATION. This warranty is void if the unit is subjected to improper or abnormal use,alteration,modification, or any form of tampering(alignment included).This warranty does not apply to damage caused by improper handling or installation.

All software is licensed on an AS-IS basis without warranty.

EXCEPT AS SPECIFICALLY PROVIDED IN THIS WARRANTY,THERE ARE NO OTHER WARRANTIES,EXPRESSED OR IMPLIED,INCLUDING BUT NOT LIMITED TO,ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL LNW RESEARCH CORPORATION BE LIABLE FOR LOSS OF PROFITS ,BENEFITS,INDIRECT ,CONSEQUENTIAL OR SIMILAR DAMAGES ARISING FROM BREACH OF THIS CONTRACT.

8/81

QUALITY ASSURANCE DEPT
LNW RESEARCH CORPORATION
262Ø WALNUT AVE
TUSTIN CA 9268Ø

ACKNOWLEDGEMENTS

TRS-80 is a trademark of TANDY CORPORATION
DOSPLUS is a product of MICROSYSTEMS SOFTWARE INC.
DBLDOS is a product of PERCOM DATA CO.
F.E.C. T8/OS is a product of FEC LTD.
LDOS is a product of LOGICAL SYSTEMS INC.
OMIKRON CP/M is a product of OMIKRON and DIGITAL RESEARCH
NEWDOS80 is a product of APPARAT INC.

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D.S.W.

K.W. 08/29/81

APPENDIX 1.Ø
USING NEWDOS8Ø VERSION 2.Ø

The NEWDOS8Ø VERSION 2.Ø system disk comes in single density format and requires that a DOUBLE DENSITY SYSTEM DISK be created using the procedure which follows. A two disk drive system is required to create the system disk. Read the section in the NEWDOS8Ø 2.Ø manual on PDRIVE specification before proceeding but do not attempt to create a double density system disk without reading these instructions.

MAKING A NEWDOS8Ø 2.Ø DOUBLE DENSITY SYSTEM DISK

1. Power the system.
2. Place a write protect tab over the notch in the NEWDOS8Ø 2.Ø Ø system disk.
3. Insert the Newdos8Ø 2.Ø disk in drive Ø.
4. Insert a blank diskette in drive 1.
5. Press RESET and boot the system.
6. Answer the date and time prompts.
7. Type:
   COPY Ø 1<ENTER>
8. Type "Y" to the FORMAT prompt and "Y" to the SYSTEM Ø prompt.Enter return<enter> to the destination prompt.
9. Move the diskette in drive 1 to drive Ø and put the NEWDOS8Ø VER 2.Ø disk in drive Ø away.Do not put a write protect tab on the newly created system disk.
10. Insert a blank diskette into drive 1.
11. After each of the following commands in STEP 12,the system will respond by listing the PDRIVE specifications for all drives and also print an error message. Wait for the NEWDOS8Ø READY prompt and then type in the next command. Do not reset the computer until instructed to. Resetting the computer with an error in the PDRIVE specifications will result in the destruction of your system diskette.
12. Type in the following commands and then return<enter>:

```
PDRIVE Ø,Ø,TI=E,TC=4Ø
PDRIVE Ø,1,TI=EK,TD=E,TC=39,SPT=18
PDRIVE Ø,2=Ø
PDRIVE Ø,3=Ø
PDRIVE Ø,4=Ø
PDRIVE Ø,5=Ø
PDRIVE Ø,6=Ø
PDRIVE Ø,7=Ø
PDRIVE Ø,8=Ø
PDRIVE Ø,9=Ø,A
```

The error message should disappear after the last entry is made. If it does not,redo the entire procedure being extra careful this time.Now the DOUBLE DENSITY system disk is to be generated:

13. Type COPY Ø 1,,CBF
    Type "Y" to format prompt and "Y" to the SYSTEM Ø prompt. Enter return<enter> to the DESTINATION DRIVE prompt.
14. When the copy is done, type DIR :1
    You should be able to verify that there are considerable more grans free on the new double density disk

than on the single density system disk in drive Ø.

15. Remove the system disk from drive Ø and replace it with the newly created double density system disk from drive 1. Press RESET and now the disk should boot up the double density disk. Type

PDRIVE Ø

Notice that the pdrive specifications for both drive 1 and drive Ø are the same (double density).

SPECIAL NOTE:

NEWDOS8Ø 2.Ø does not have automatic density recognition as does DOSPLUS 3.3d and the zaps from CIRCLE J. This means that if you would like to look at the directory or copy files to and from or execute a file from a single density diskette you cannot do it without first changing the PDRIVE specifications on your NEWDOS8Ø 2.Ø drive Ø disk. This can be done as follows:

PDRIVE Ø,1=3,A

This assumes that drive 1 is the drive that the single density disk will be inserted into. To change back to double density on drive 1 simply type:

PDRIVE Ø,1=Ø,A

This sets (or equates) the pdrive specifications for drive 1 to be the same as drive Ø (double density).

APPENDIX 2.0 SA800 DISK DRIVE OPTION SELECTIONS

CUSTOMER INSTALLABLE OPTIONS

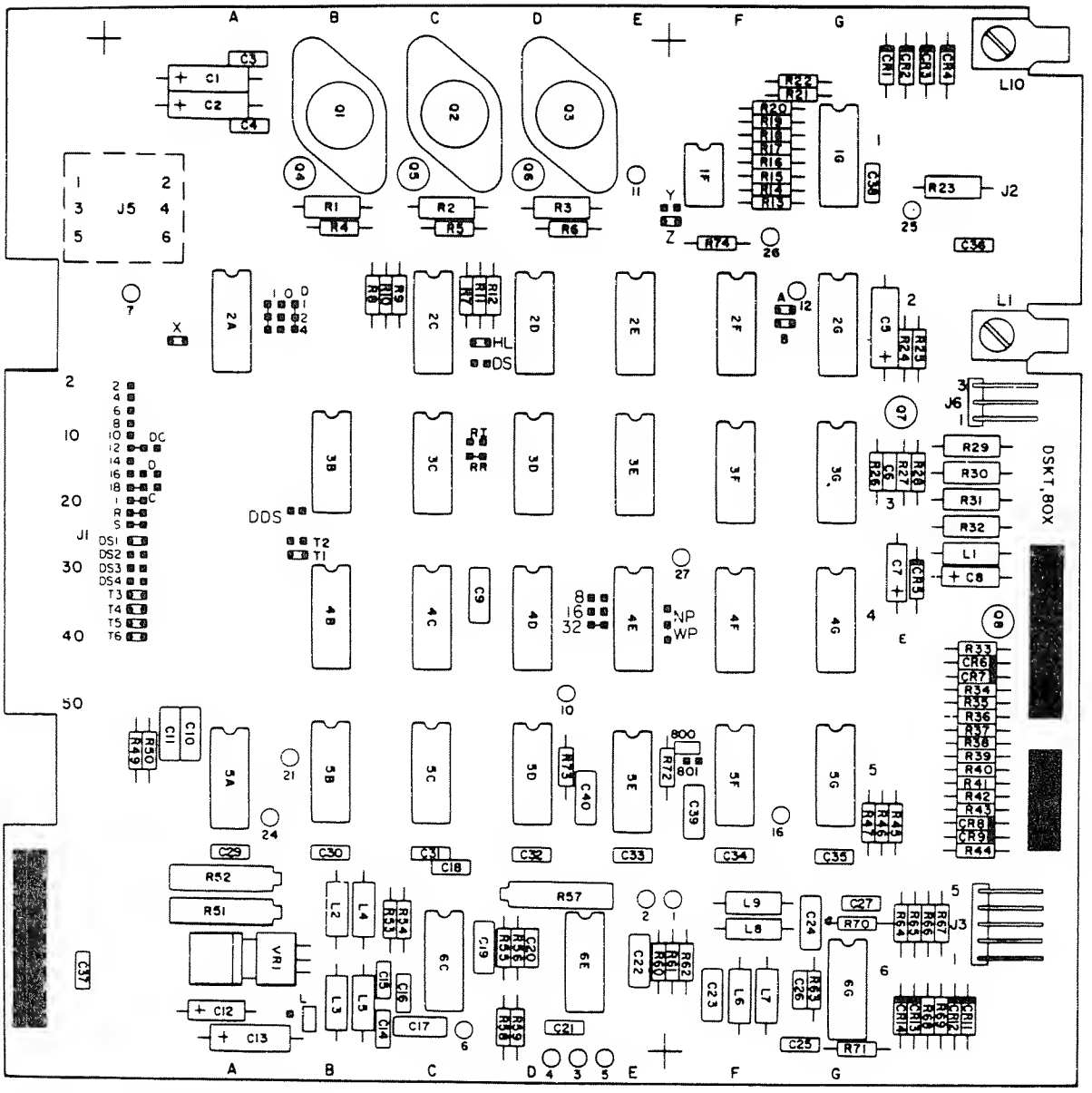
The SA800/801 can be modified by the user to function differently than the standard method as outlined in sections 3 and 4. These modifications can be implemented by adding or deleting traces and by use of the Alternate I/O pins. Some traces are capable of being connected by use of a shorting plug, Shugart P/N 15648 or AMP P/N 530153-2. This section will discuss a few examples of modifications and how to install them. The examples are:

1. Drive Select one to eight drives.
2. Select drive without loading head or enabling stepper.
3. Select drive and enable stepper without loading the head.
4. Load head without selecting drive or enabling stepper.
5. Radial Ready.
6. Radial Index/Sector.
7 Eight, 16, or 32 Sector option.
8. In Use (Activity L.E.D.) optional input.
9. Write Protect options.

Tabulated below are the trace options with the condition of the trace as it is shipped from the factory. Figure 21 shows the location of these traces on the PCB.

CUSTOMER CUT/ADD TRACE OPTIONS

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
T3,T4,T5,T6	Terminations for Multiplexed Inputs		Plugged
T1	Terminator for Drive Select		Plugged
T2	Spare Terminator for Radial Head Load	X	
DS1,DS2,DS3,DS4	Drive Select Input Pins	X	DS1 is Plugged
RR	Radial Ready		X
RI	Radial Index and Sector		X
R,I,S	Ready, Index, Sector Alternate Output Pads		X
HL	Stepper Power From Head Load		Plugged
DS	Stepper Power From Drive Select	X	
WP	Inhibit Write When Write Protected		X
NP	Allow Write When Write Protected	X	
8,16,32	8, 16, 32 Sectors (SA801 Only)	8 & 16	32
D	Alternate Input-In Use	X	
2,4,6,8,10,12,14,16,18	Nine Alternate I/O Pins	X	
D1,D2,D4,DDS	Customer Installable Decode Drive Select Option	X	
A,B,X	Radial Head Load		Plugged
C	Alternate Input-Head Load	X	
Z	In Use from Drive Select		Plugged
Y	In Use from HD LD	X	
DC	Alternate Output-Disk Change	X	
NFO	Non Force Out	X	
TS	True FM Data Separation	X	



Jumper Plug Installed as Shipped

Test Point

Component Locations Standard PCB